

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MBP 15 "MLB

08/18/2008

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N/A

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N/A

N/A

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DDR

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N/A

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(MASTER)

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(MASTER)

(MASTER)

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01/22/2008

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

DATE

ENG APPD

DATE

?

?

?

?

?

?

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7546	1	SCHEM,FIBBO,M98	SCH	CRITICAL	
820-2330	1	PCBF,FIBBO,M98	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST_MODIFIED=Mon Aug 18 01:48:34 2008

DIMENSIONS ARE IN MILLIMETERS

XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

DESIGN CK

MFG APPD

DESIGNER

SCALE

NONE

MATERIAL/FINISH

NOTED AS

APPLICABLE

SIZE

D

DRAWING NUMBER

051-7546

REV.

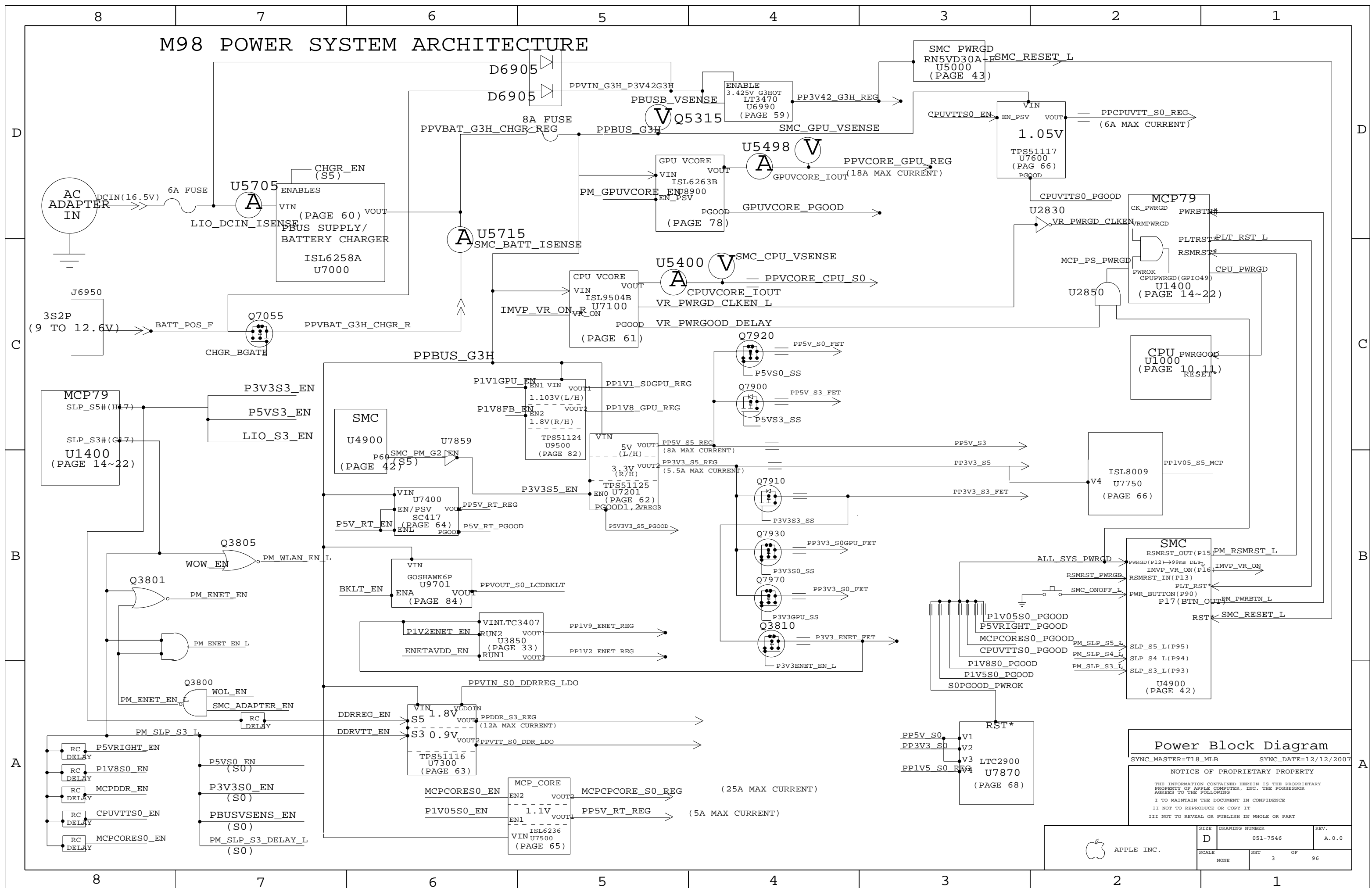
A.0.0

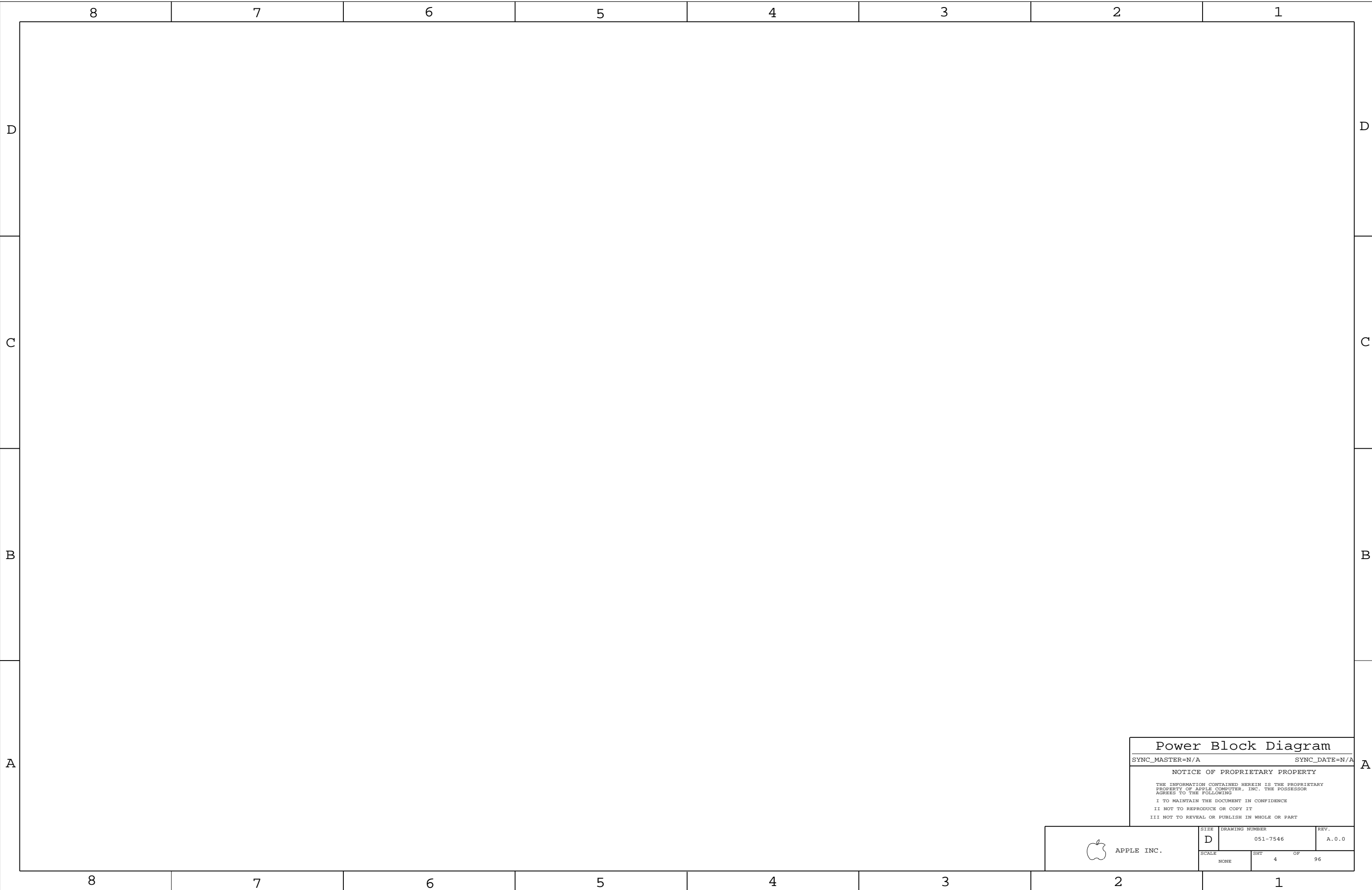
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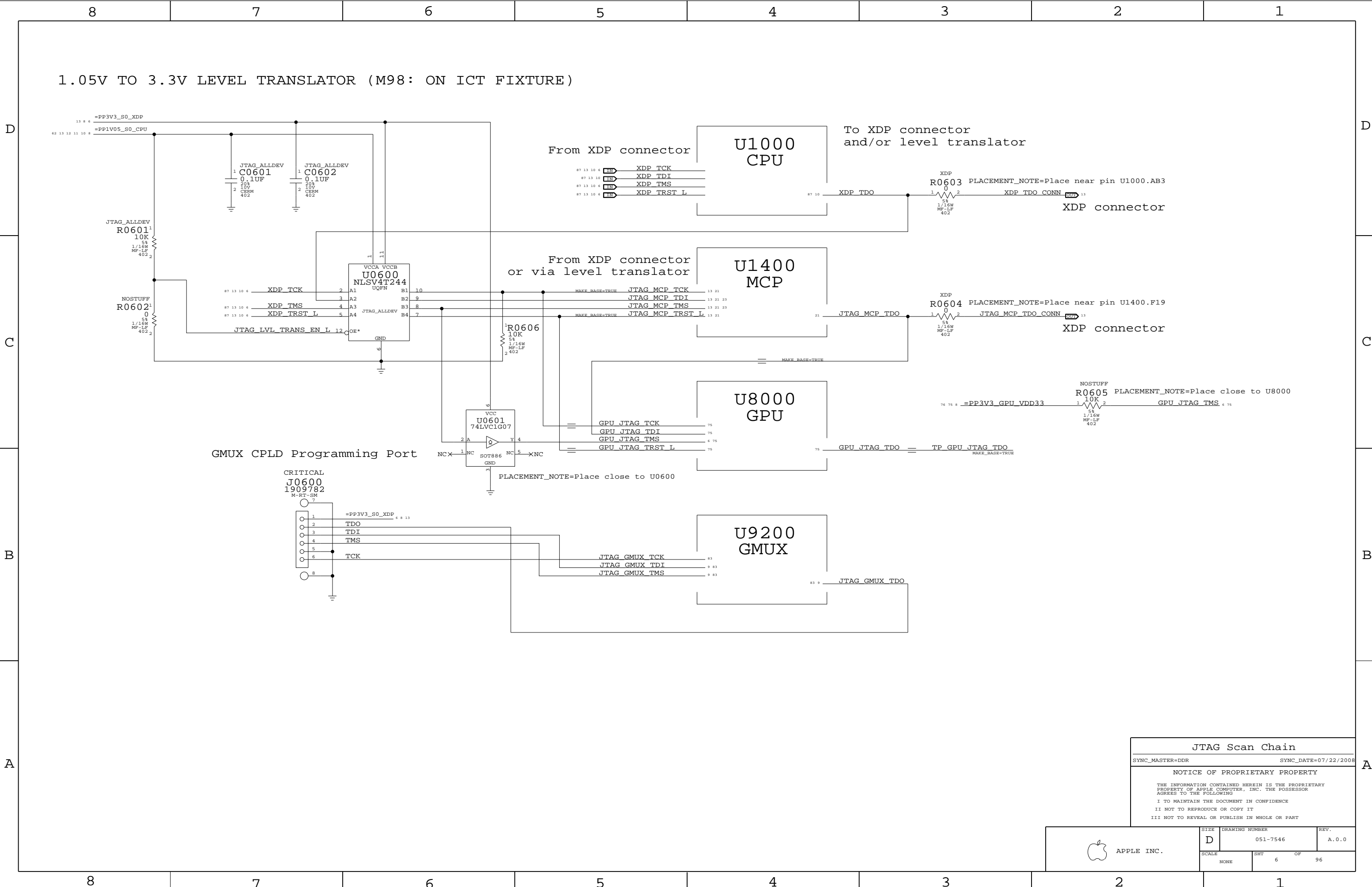




Power Block Diagram		
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D	051-7546	A.0.0
SCALE	SHT 4 OF 96	
NONE		

	APPLE INC.
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8		7		6		5		4		3		2		1	
BOM Variants															
BOM NUMBER		BOM NAME				BOM OPTIONS									
630-9334		PCBA, 2.4GHZ, 256SAM_VRAM, M98				M98_COMMON,EEE_OZA,CPU_2_4GHZ,FB_256_SAMSUNG									
630-9335		PCBA, 2.4GHZ, 256HYN_VRAM, M98				M98_COMMON,EEE_OZB,CPU_2_4GHZ,FB_256_HYNIX									
630-9336		PCBA, 2.5GHZ, 512SAM_VRAM, M98				M98_COMMON,EEE_OZC,CPU_2_5GHZ,FB_512_SAMSUNG									
630-9337		PCBA, 2.5GHZ, 512QIM_VRAM, M98				M98_COMMON,EEE_OZD,CPU_2_5GHZ,FB_512_QIMONDA									
630-9585		PCBA, 2.8GHZ, 512SAM_VRAM, M98				M98_COMMON,EEE_2NH,CPU_2_8GHZ,FB_512_SAMSUNG									
630-9586		PCBA, 2.8GHZ, 512QIM_VRAM, M98				M98_COMMON,EEE_2NJ,CPU_2_8GHZ,FB_512_QIMONDA									
M98 BOM Groups															
BOM GROUP		BOM OPTIONS													
M98_COMMON		ALTERNATE,COMMON,M98_COMMON1,M98_COMMON2,M98_COMMON3,M98_DEBUG,M98_PROGPARTS													
M98_COMMON1		ONEWIRE_PU,ISL6258A,MEMRESET_HW,MEMRESET_MCP,MCP_B02,MCP_PROD,MCPSEQ_SMC													
M98_COMMON2		BKLT_PLL_NOT,BMON_ENG,MIKEY,BOOT_MODE_USER,GPUVID_1P00V,MUXGFX													
M98_COMMON3		DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_HW,DP_CA_DET_EG_PLD,MCP_CS1_NO													
M98_DEBUG		SMC_DEBUG_YES,XDP,LPCPLUS,VREFMRGN													
M98_PROGPARTS		GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG													
BOM GROUP		BOM OPTIONS													
FB_256_SAMSUNG		VRAM4,VRAM_256_SAMSUNG													
FB_256_HYNIX		VRAM4,VRAM_256_HYNIX													
FB_512_SAMSUNG		VRAM4,VRAM_512_SAMSUNG													
FB_512_QIMONDA		VRAM4,VRAM_512_QIMONDA													
Bar Code Labels / EEE #'s															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:OZA]		CRITICAL		EEE_OZA					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:OZB]		CRITICAL		EEE_OZB					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:OZC]		CRITICAL		EEE_OZC					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:OZD]		CRITICAL		EEE_OZD					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:2NH]		CRITICAL		EEE_2NH					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:2NJ]		CRITICAL		EEE_2NJ					
Module Parts															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION					
337S3639		1	IC,PDC,SLB4N,PRQ,2.4G,25W,1066,M0,3M,BGA			U1000		CRITICAL		CPU_2_4GHZ					
337S3640		1	IC,PDC,SL3BX,PRQ,2.53G,35W,1066,C0,6M,BGA			U1000		CRITICAL		CPU_2_5GHZ					
338S0554		1	IC,GPU,55nm,NV G96-GS,BGA969,LF			U8000		CRITICAL							
338S0570		1	IC,RTL8211CL,GIGE TRANSCEIVER,48P TQFP			U3700		CRITICAL							
338S0523		1	IC,PW643-06,1394B PHY/ONCI LINK/PCI-E,12			U4100		CRITICAL							
338S0600		1	IC,GMCP,MCP79-B01,35x35MM,BGA1437			U1400		CRITICAL		MCP_B01					
338S0563		1	IC,SMC,HS8/2117,9MMX9MM,TLP			U4900		CRITICAL		SMC_BLANK					
341S2289		1	IC,SMC,DEVELOPMENT,M98			U4900		CRITICAL		SMC_PROG					
335S0384		1	IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8			U6100		CRITICAL		BOOTROM_BLANK					
341S2366		1	IC,EFI ROM,DEVELOPMENT,M98			U6100		CRITICAL		BOOTROM_PROG					
341S2272		1	IC,HDCP ROM,NVG96, 8 PIN SOIC,LF,HF			U8770		CRITICAL		HDCP_YES					
341S2384		1	IR,ENCORE II, CY7C63803-LQXC			U4800		CRITICAL							
338S0635		1	IC,GMCP,MCP79-B02,35x35MM,BGA1437			U1400		CRITICAL		MCP_B02					
341S2383		1	IC,PSOC +W/USB,56PIN,MLF,M98			U5701		CRITICAL		TPAD_PROG					
337S3641		1	IC,PDC,SLB43,PRQ,2.8G,35W,1066,C0,6M,BGA			U1000		CRITICAL		CPU_2_8GHZ					
333S0482		4	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA			U8400,U8450,U8500,U8550		CRITICAL		VRAM_256_SAMSUNG					
333S0483		4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA			U8400,U8450,U8500,U8550		CRITICAL		VRAM_256_HYNIX					
333S0481		4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA			U8400,U8450,U8500,U8550		CRITICAL		VRAM_512_SAMSUNG					
333S0472		4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA			U8400,U8450,U8500,U8550		CRITICAL		VRAM_512_QIMONDA					
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:										
138S0603		138S0602		ALL	Murata alt to Samsung										
353S1681		353S1294		ALL	ONY011,ONAMP, GMS										
152S0276		152S0683		ALL	Maplayers alt to Delta/Vishay										
341S2367		341S2366		ALL	Macromia alt to SST										
152S0876		152S0867		ALL	Maplayer alt to Delta										
157S0058		157S0055		ALL	Delta alt to TDK Magnetics										
353S2312		353S1466		ALL	INTERSEIL ALT TO INTERSEIL										
514-0612		514-0607		ALL	FOXLINK RCVR ALT TO FOMCONB										
514-0613		514-0608		ALL	FOXLINK RCVR ALT TO FOMCONB										
152S0915		152S0796		ALL	Maplayers alt to Cytacoe IMD										
BOM Configuration															
SYNC_MASTER=N/A SYNC_DATE=N/A															
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JTAG Scan Chain

SYNC_MASTER=DDR

SYNC_DATE=07/22/2008


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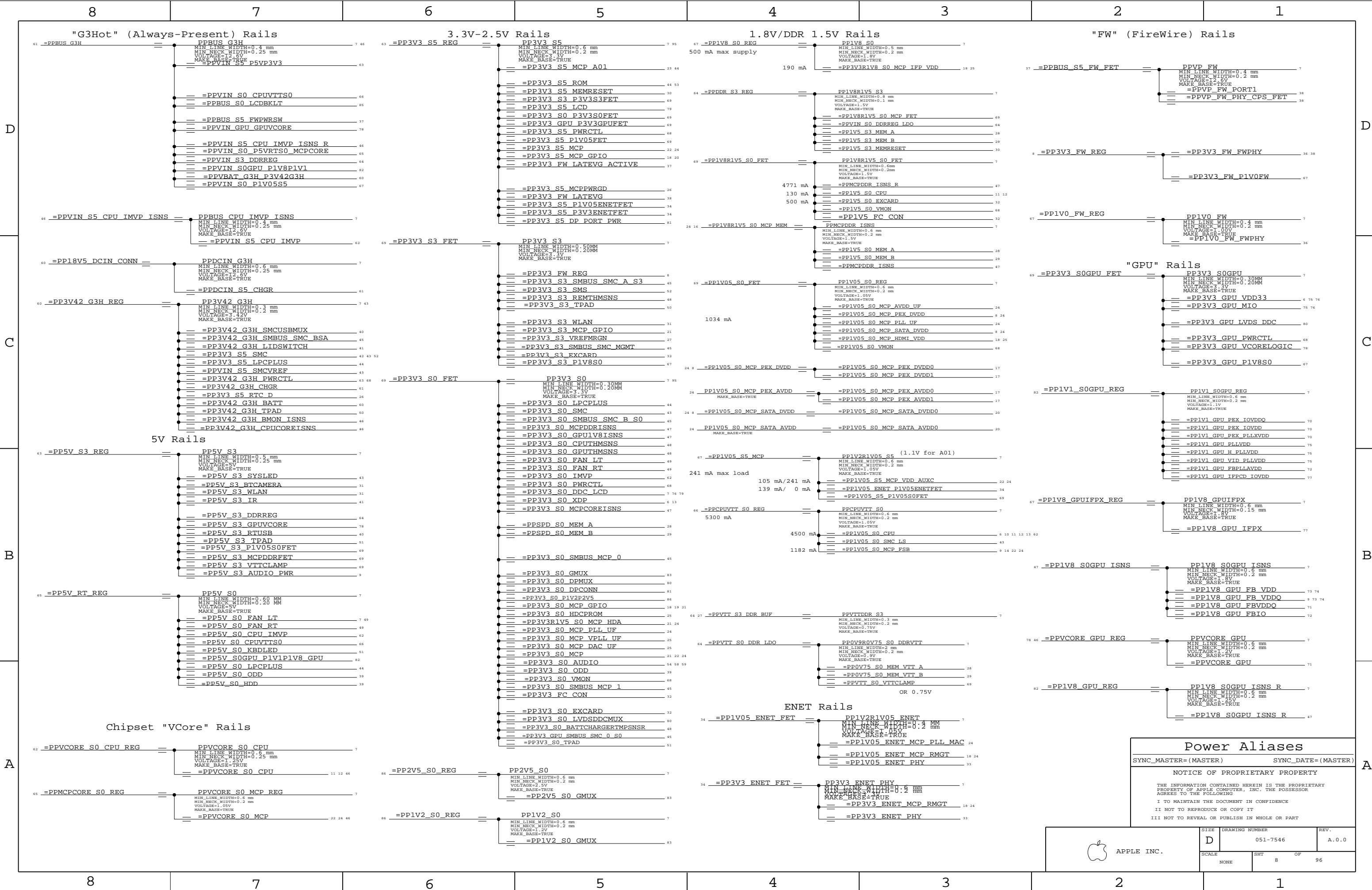
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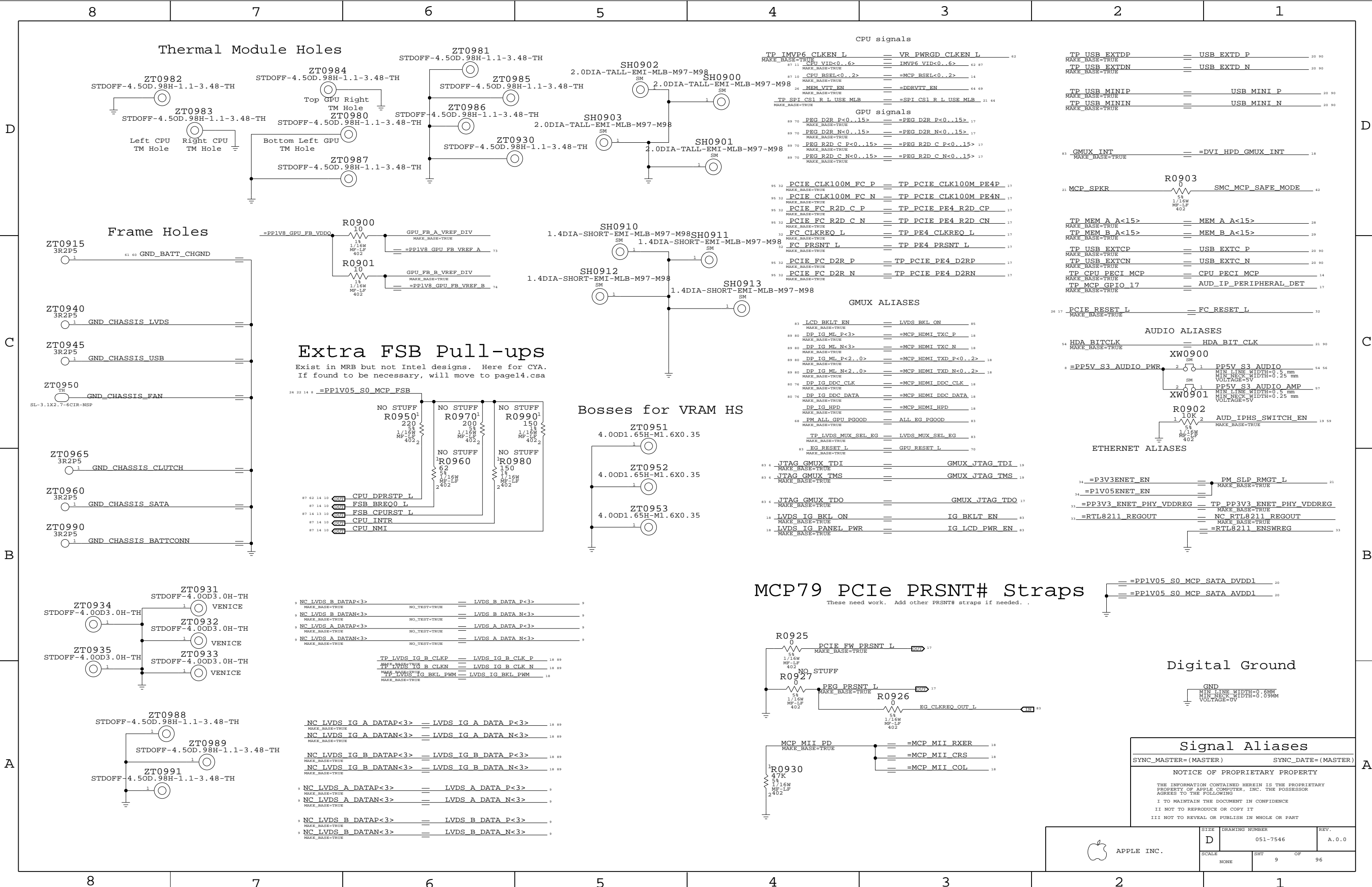
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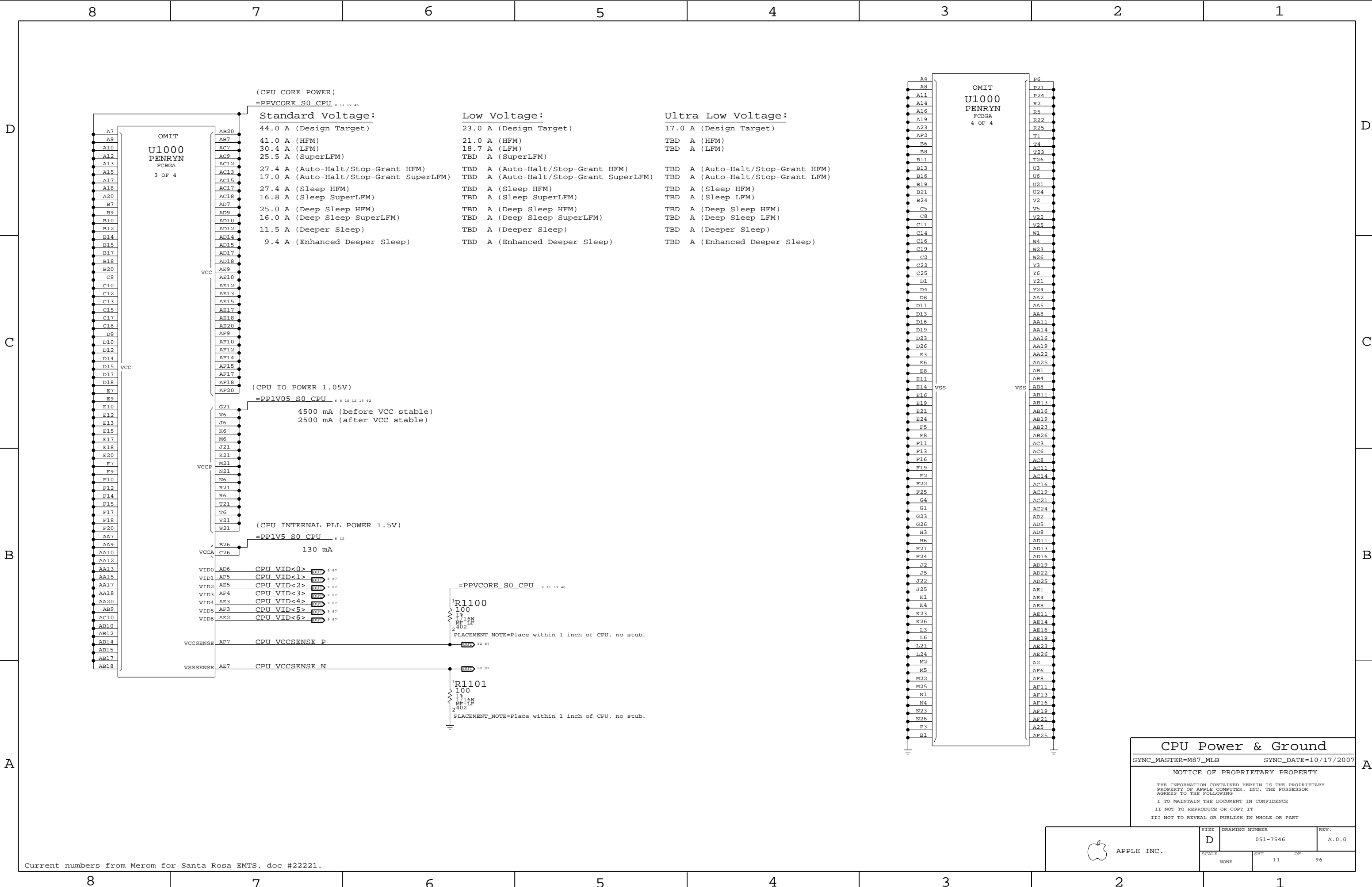
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CPU Power & Ground

SYNC_MASTER=M87_MLB

SYNC_DATE=10/17/2007


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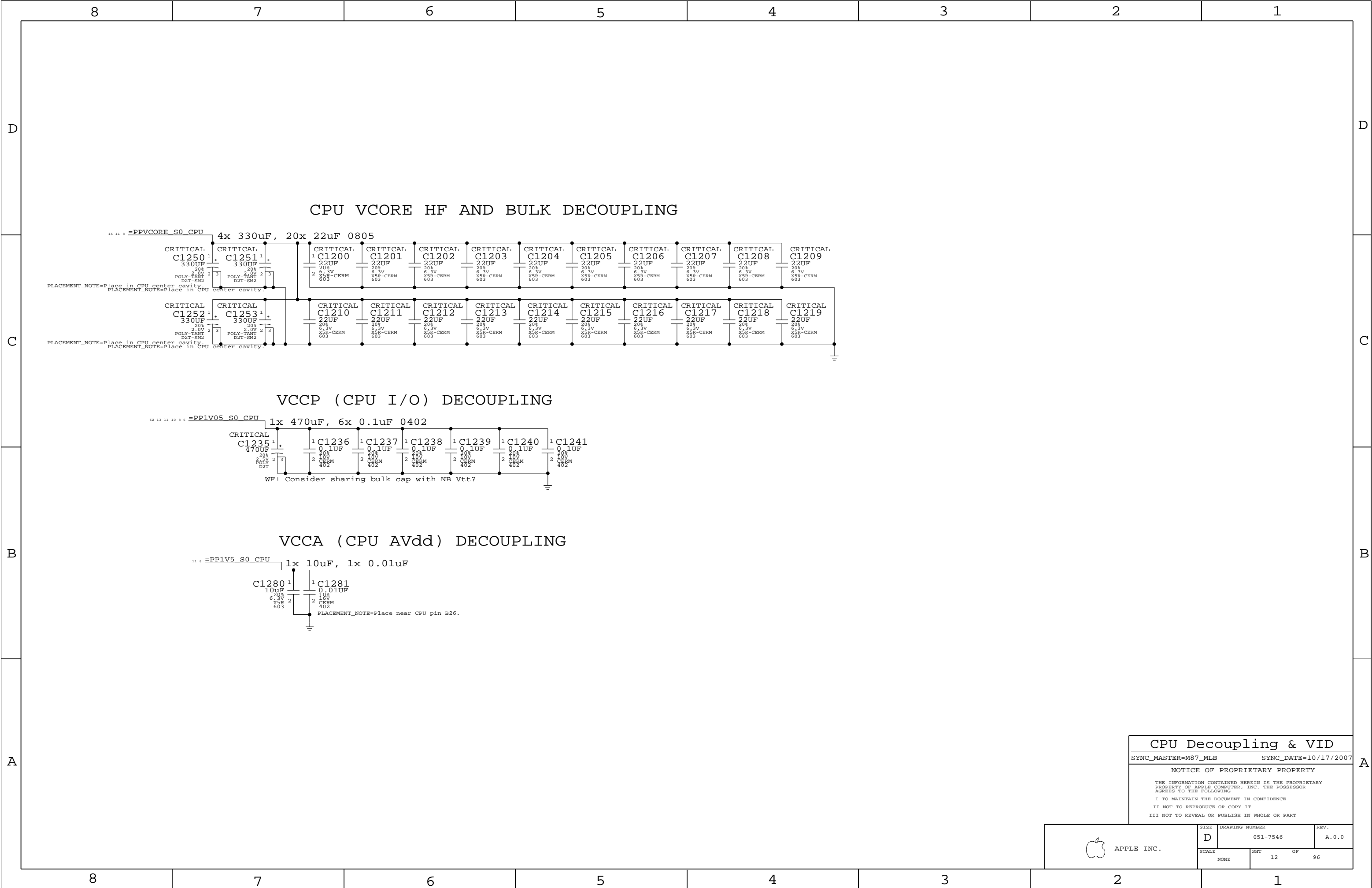
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NONE		11	96



D

D

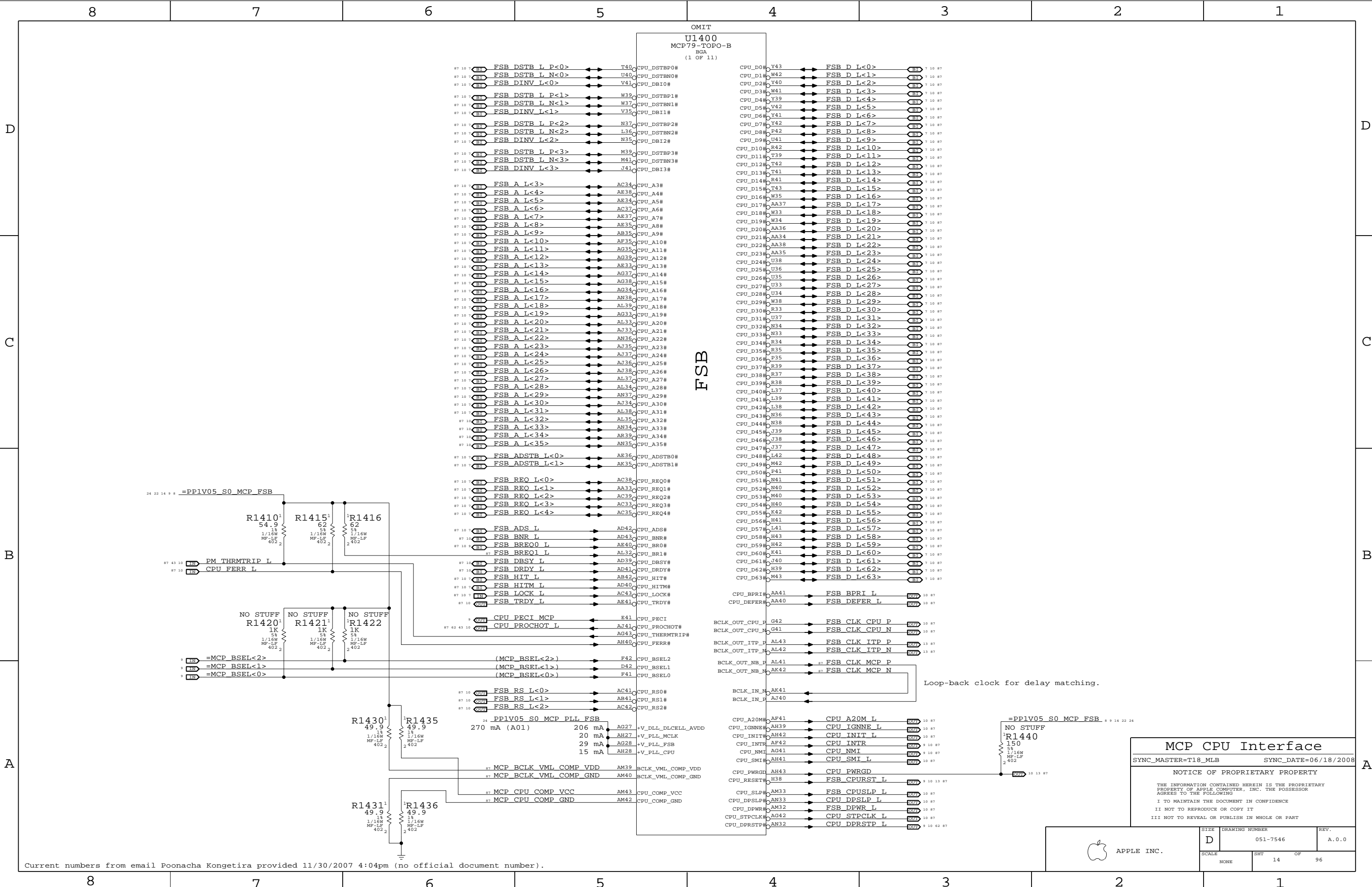
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B

B

A



MCP CPU Interface

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008

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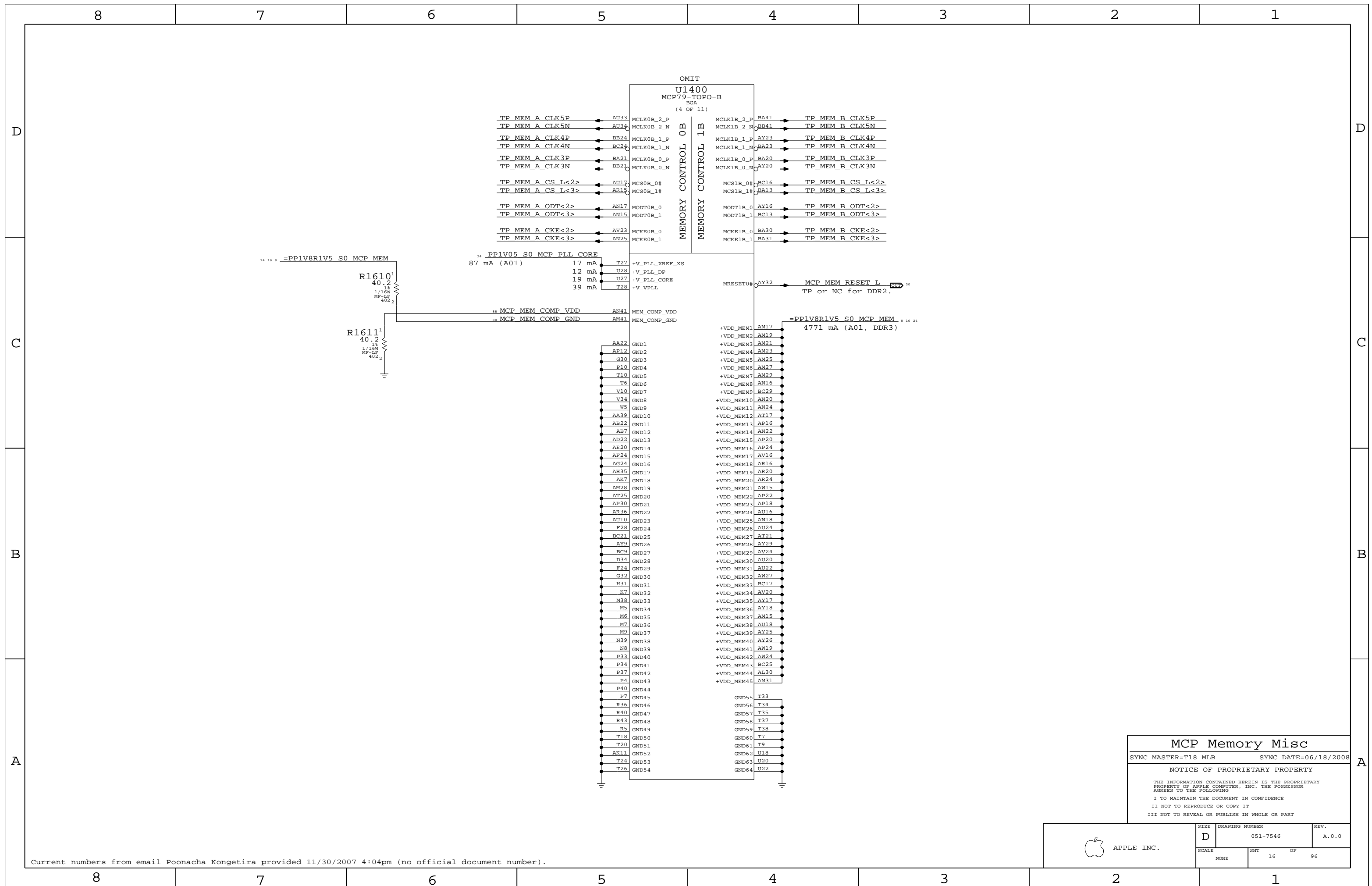
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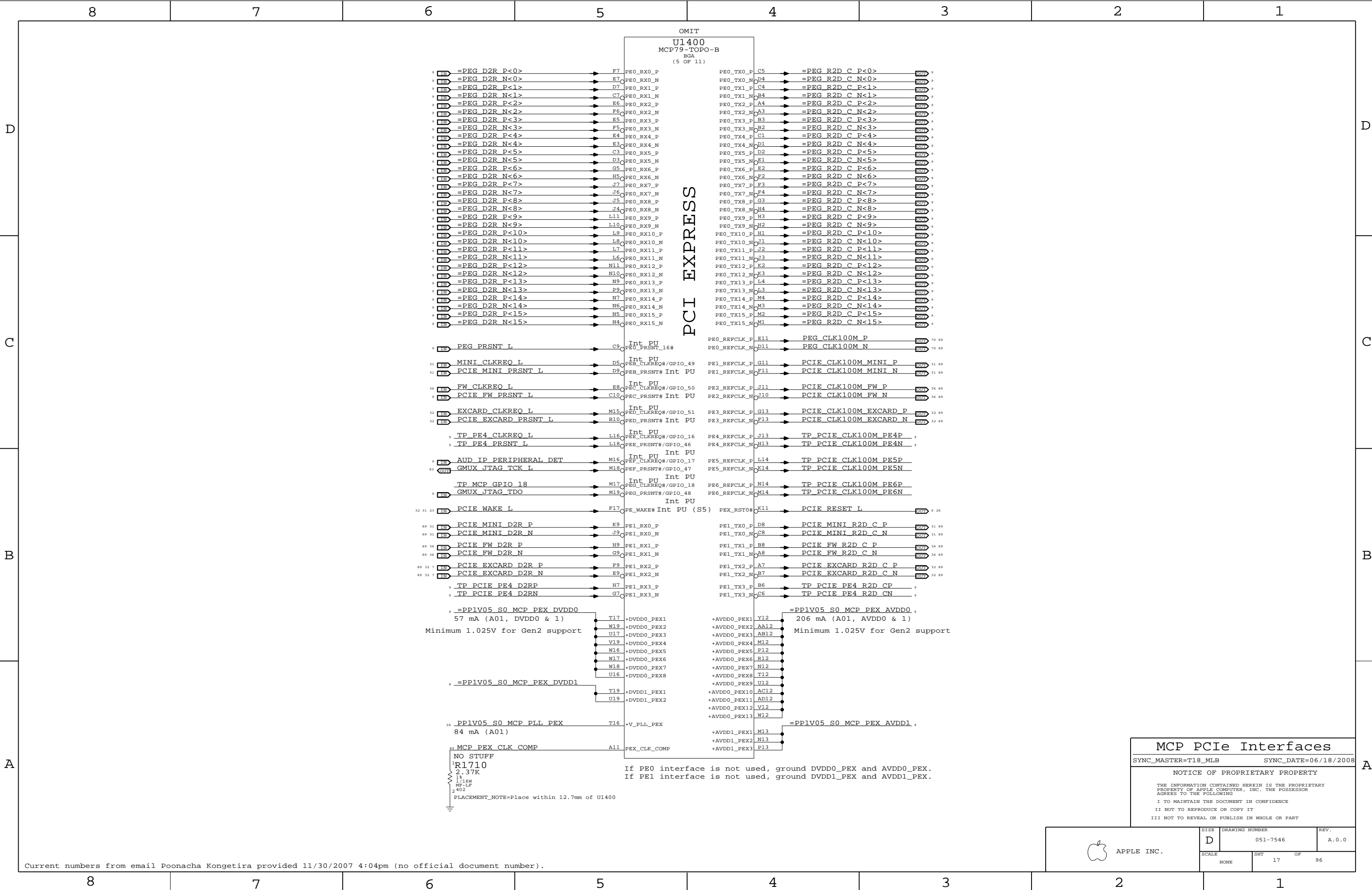
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SCALE		SHT	OF
NONE		14	96







MCP PCIe Interfaces

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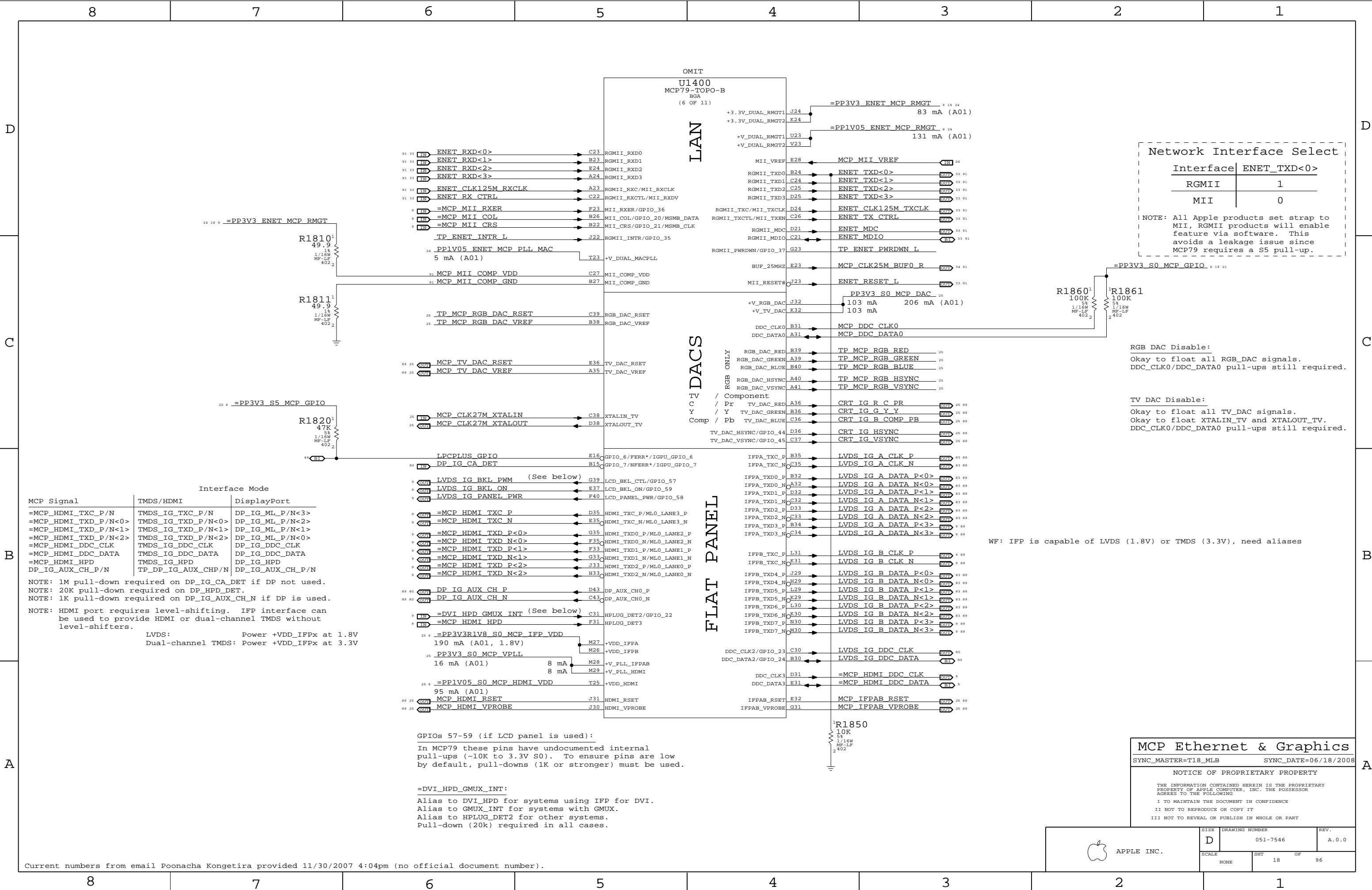
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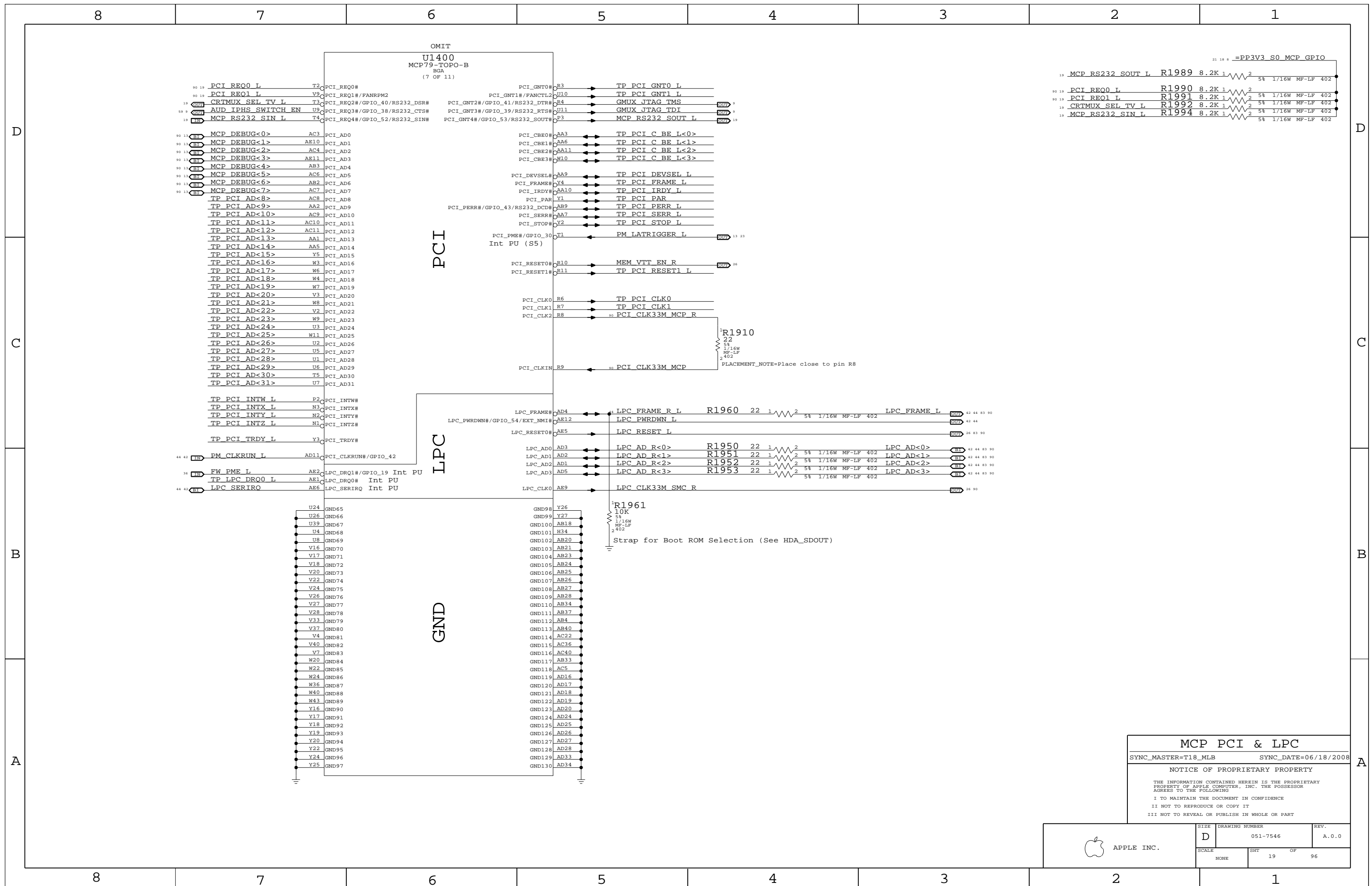
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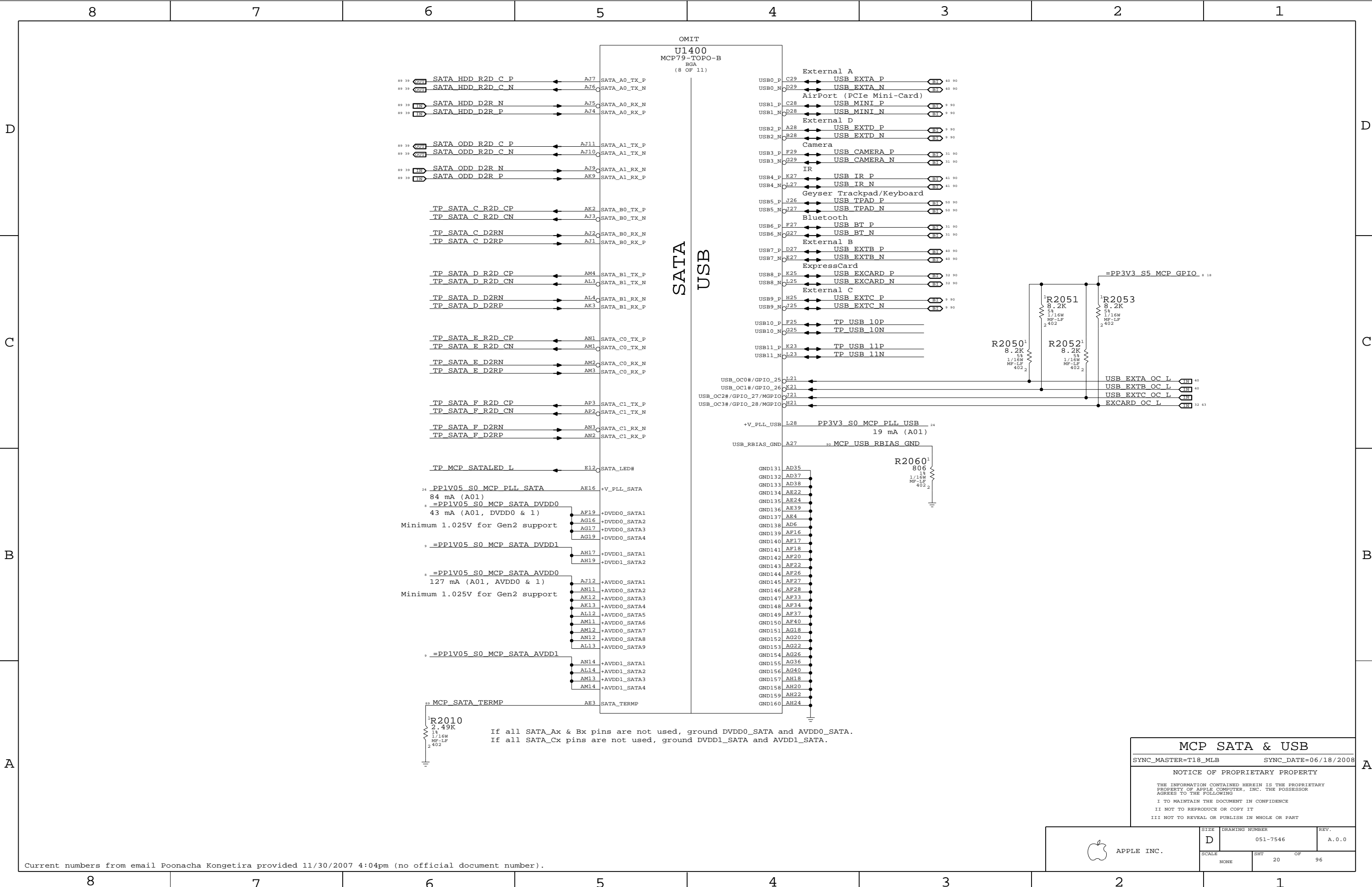


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	17	96







MCP SATA & USB

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008


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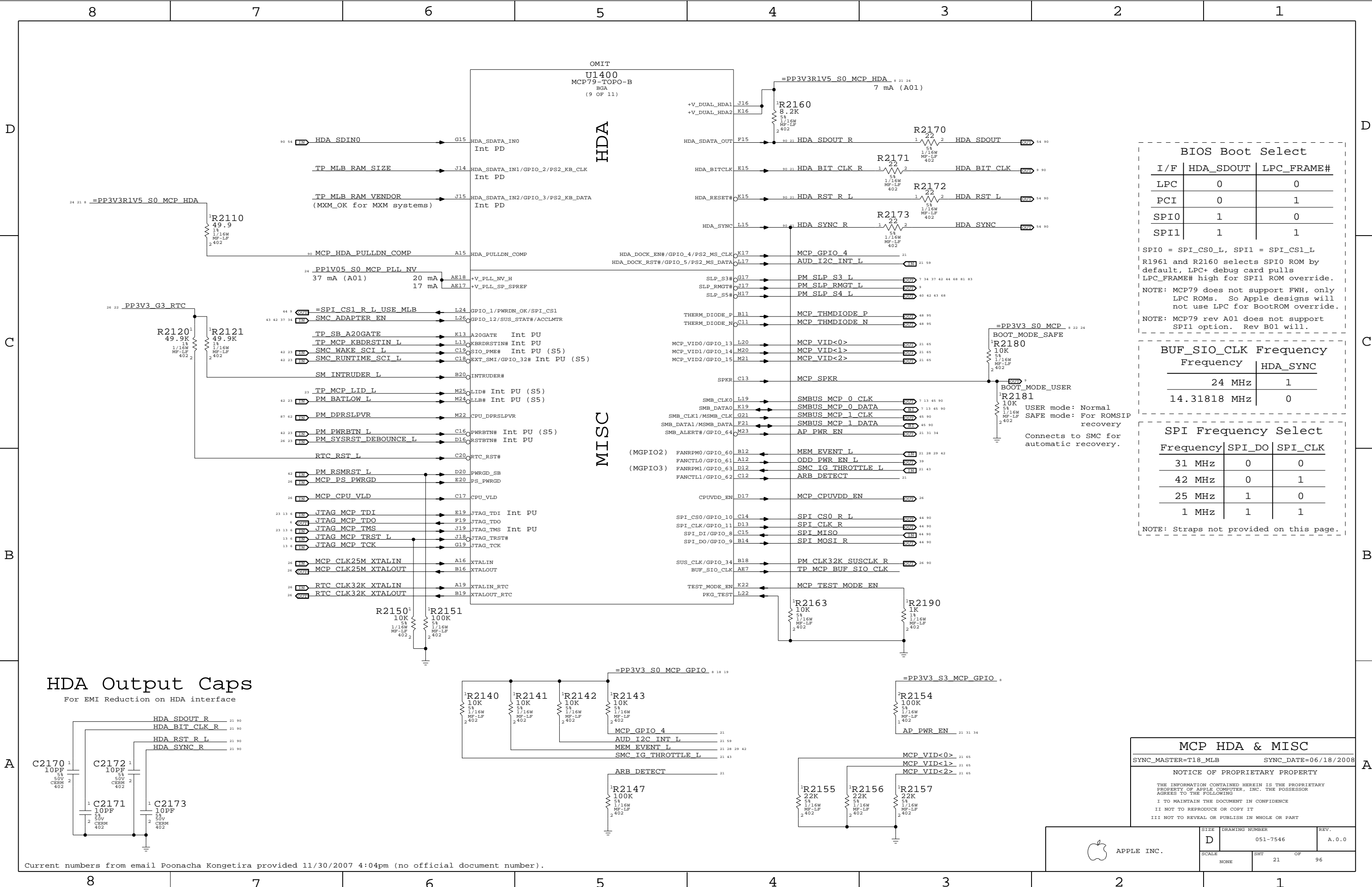
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SCALE		SHT	OF
NONE		20	96



BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

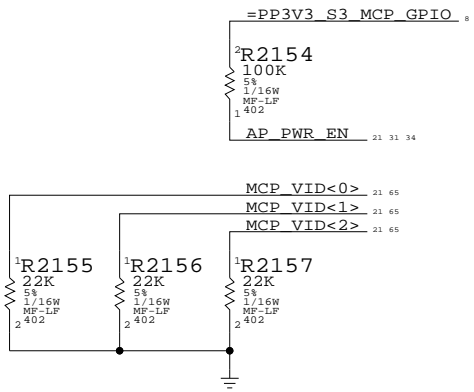
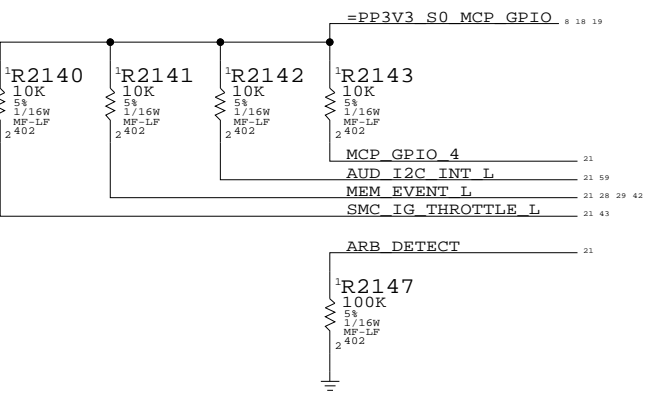
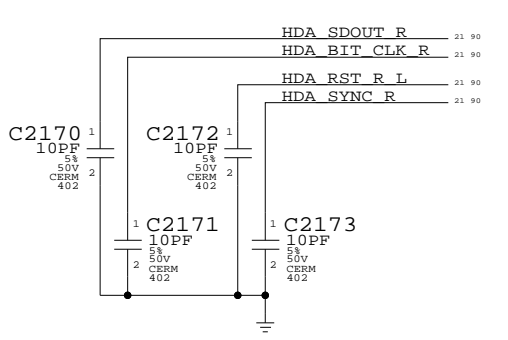
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

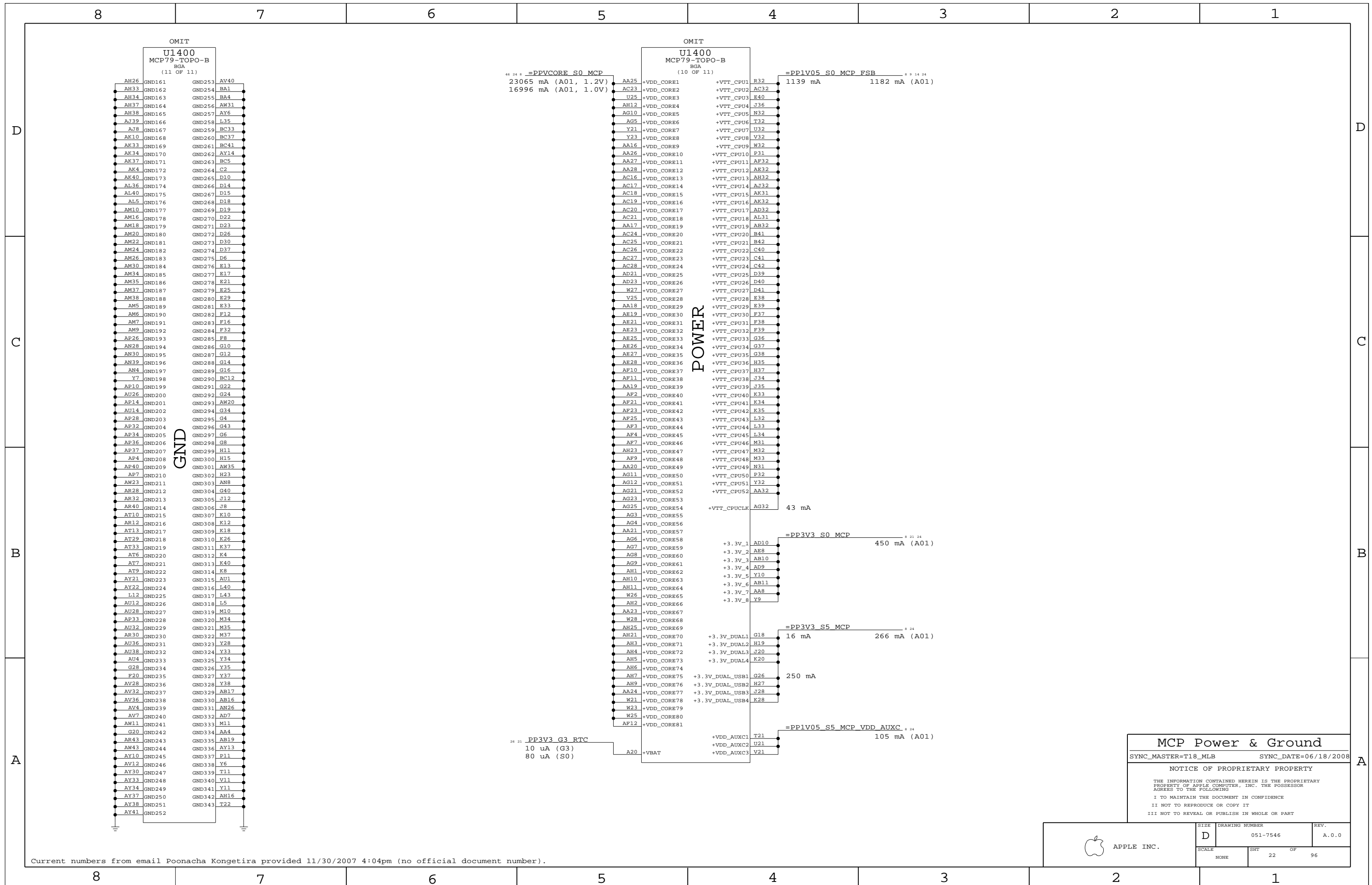
HDA Output Caps

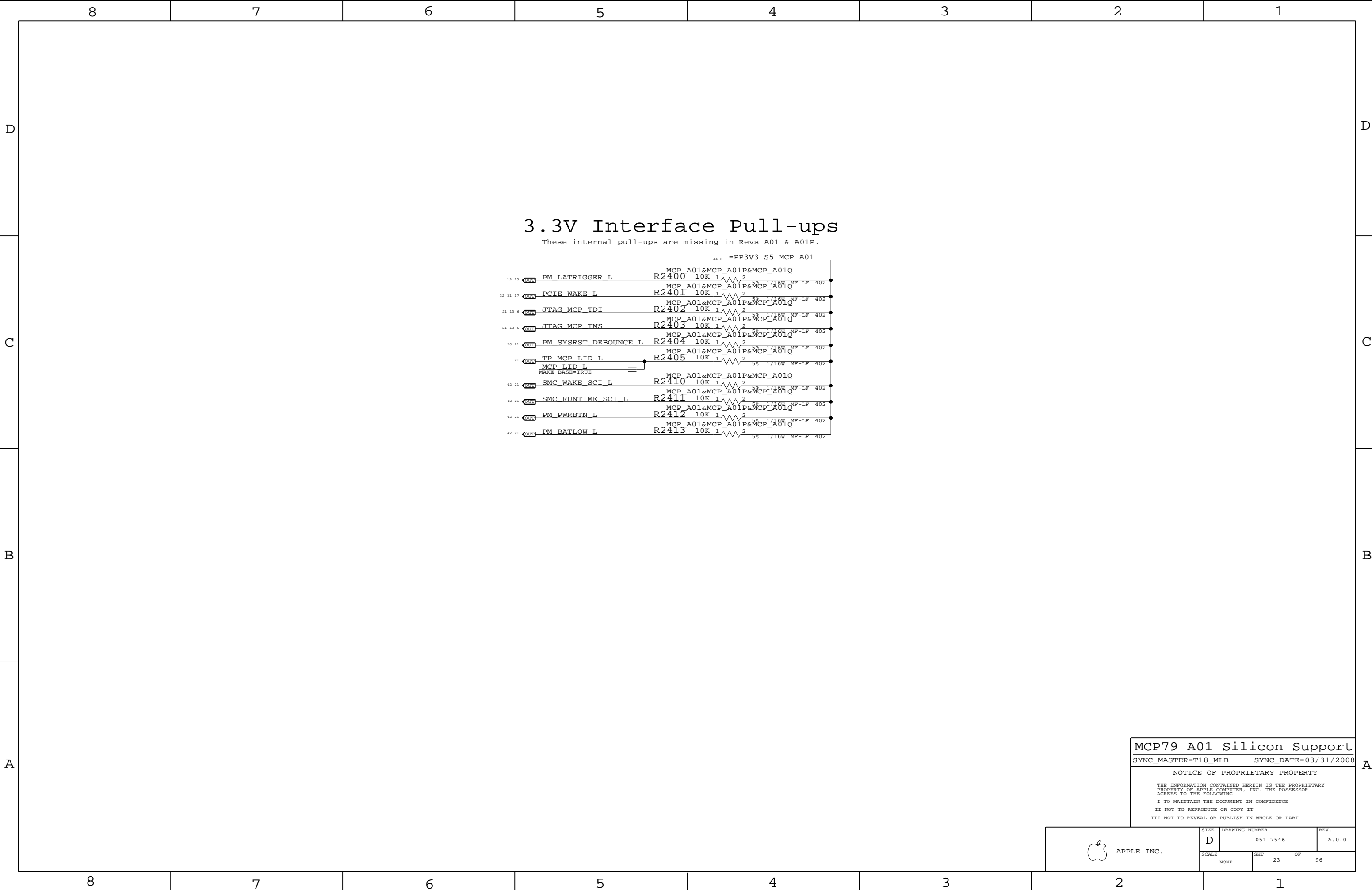
For EMI Reduction on HDA interface



MCP HDA & MISC		
SYNC_MASTER=T18_MLB		SYNC_DATE=06/18/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		21	96





MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

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SCALE

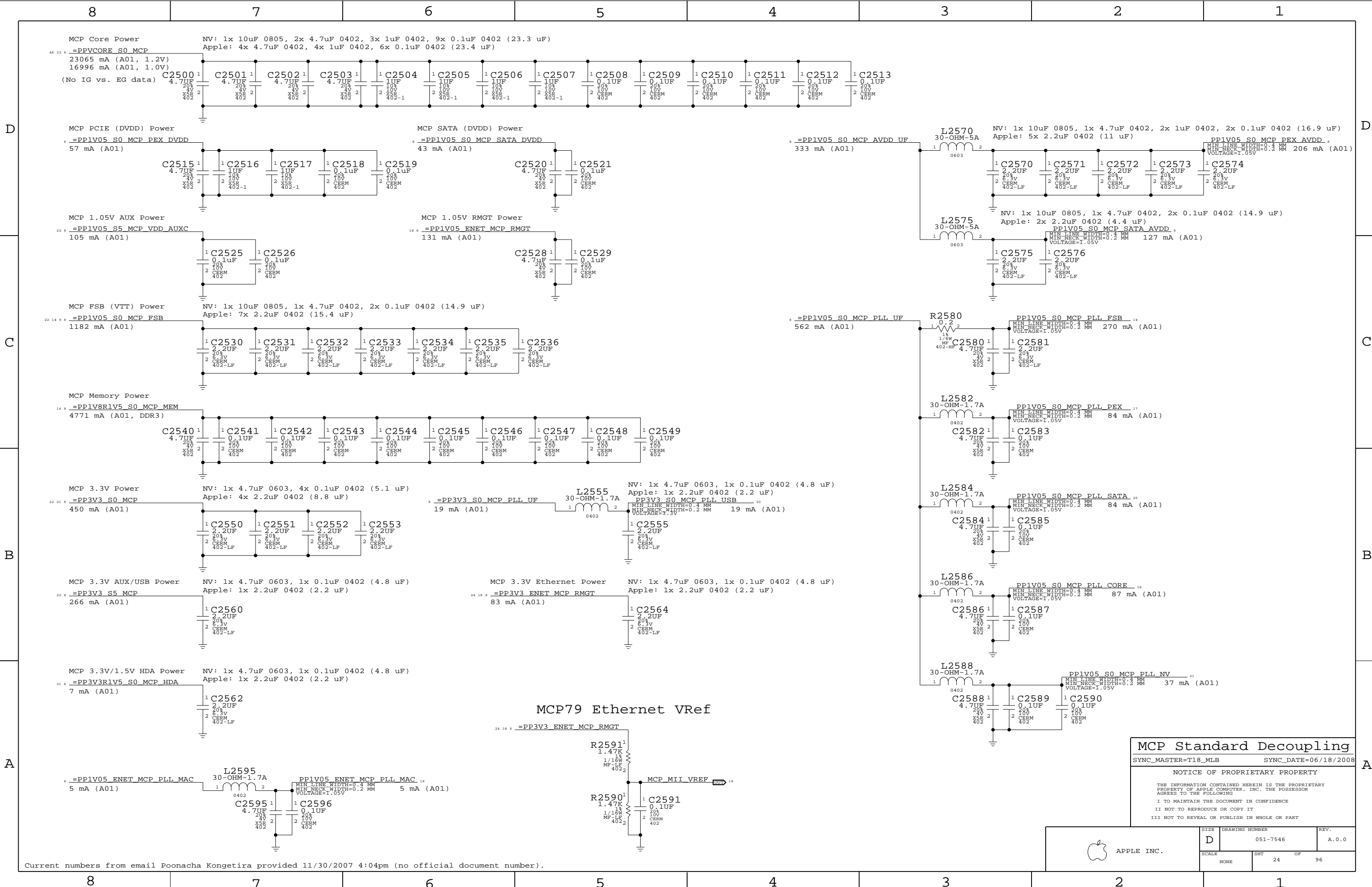
NONE

SHT

23

OF

96



Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM A VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

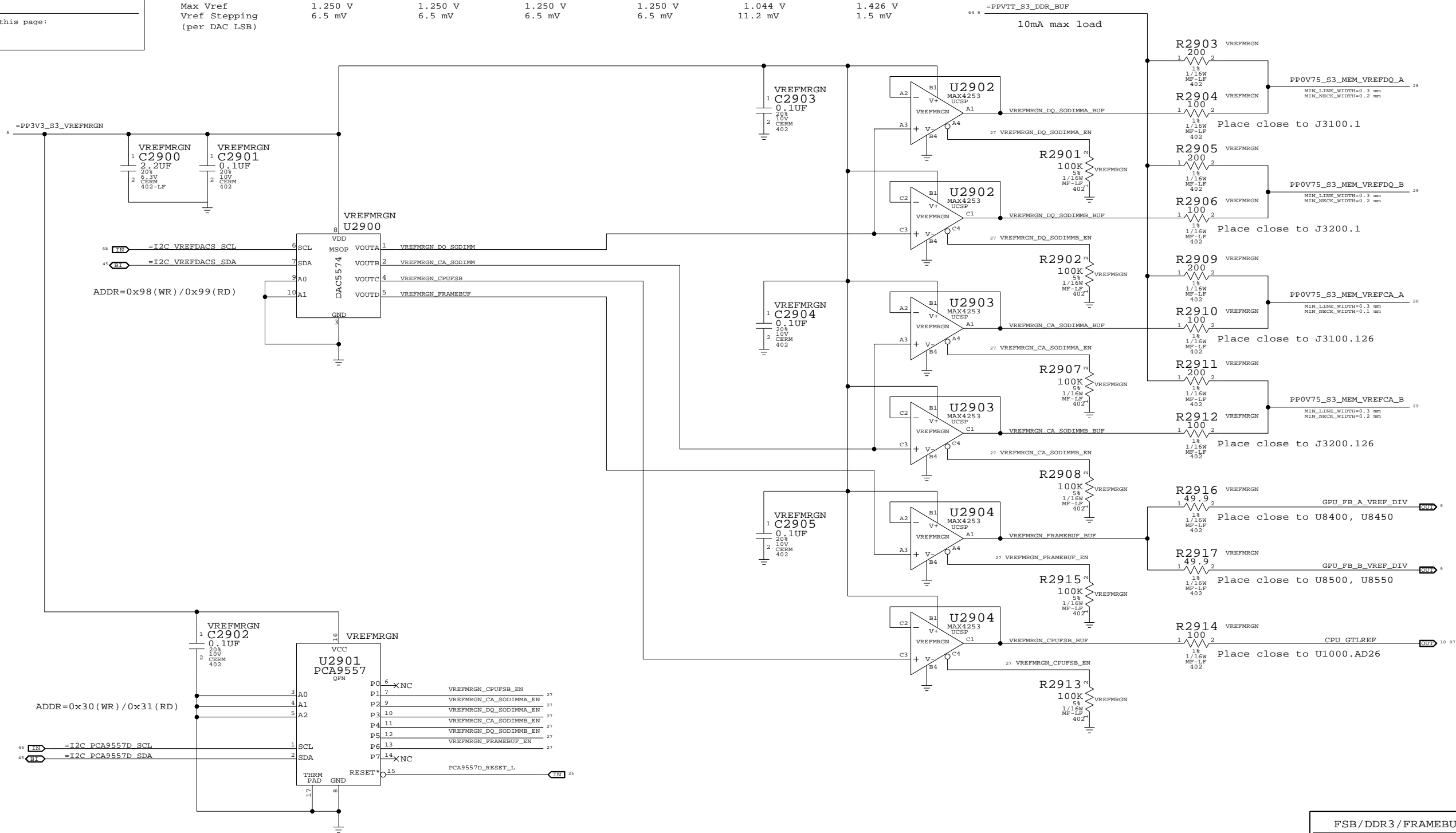
MEM B VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM B VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

CPU FSB VREF
C
0x00
0x55
-0.91 mA
0.52 mA
0.70 V
0.091 V
1.044 V
11.2 mV

FRAME BUFFER VREF
D
0x00
0xFF
-59.04 mA
51.15 mA
1.248 V
1.042 V
1.426 V
1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

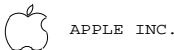
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

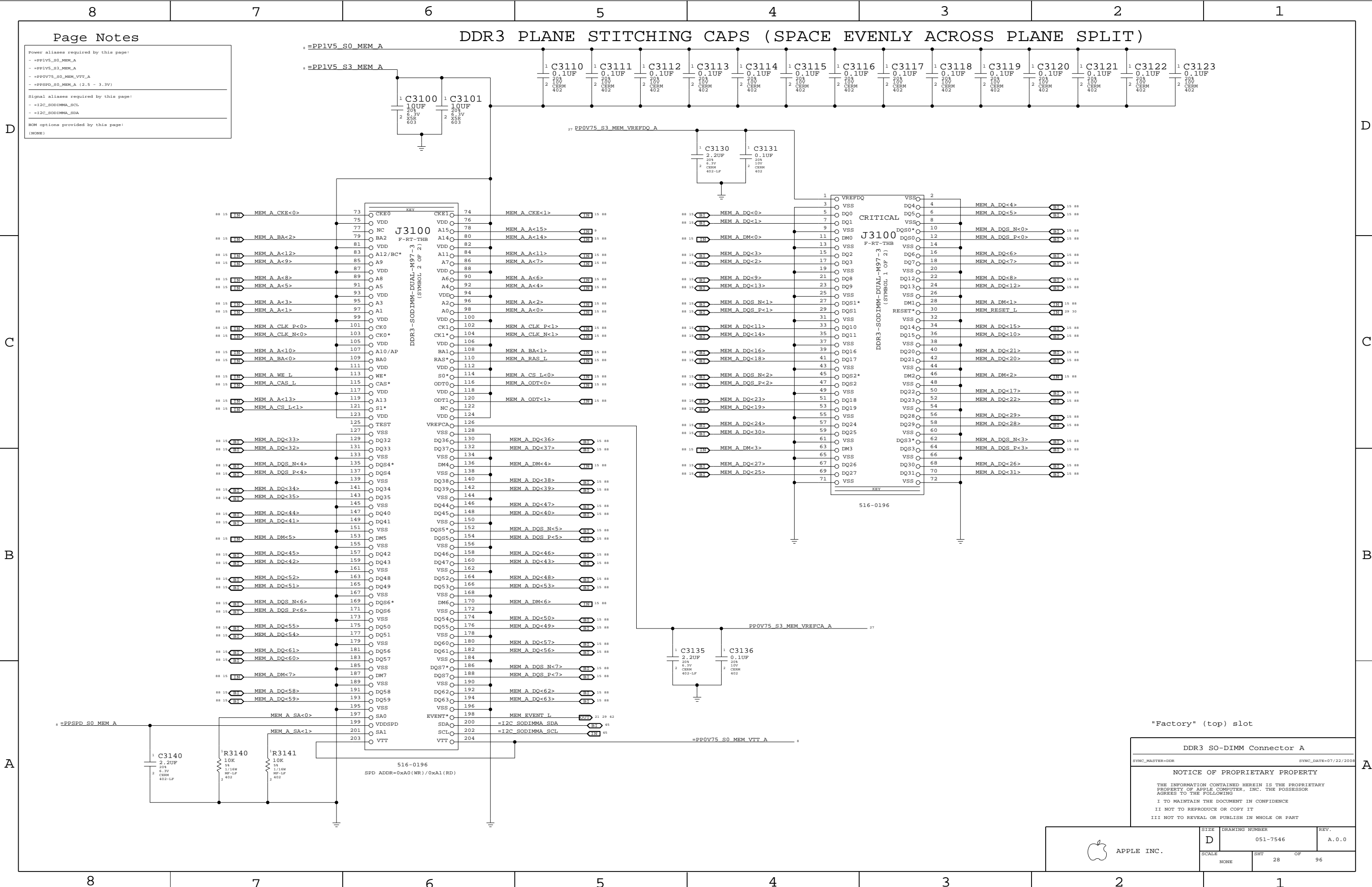
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	27	96



Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

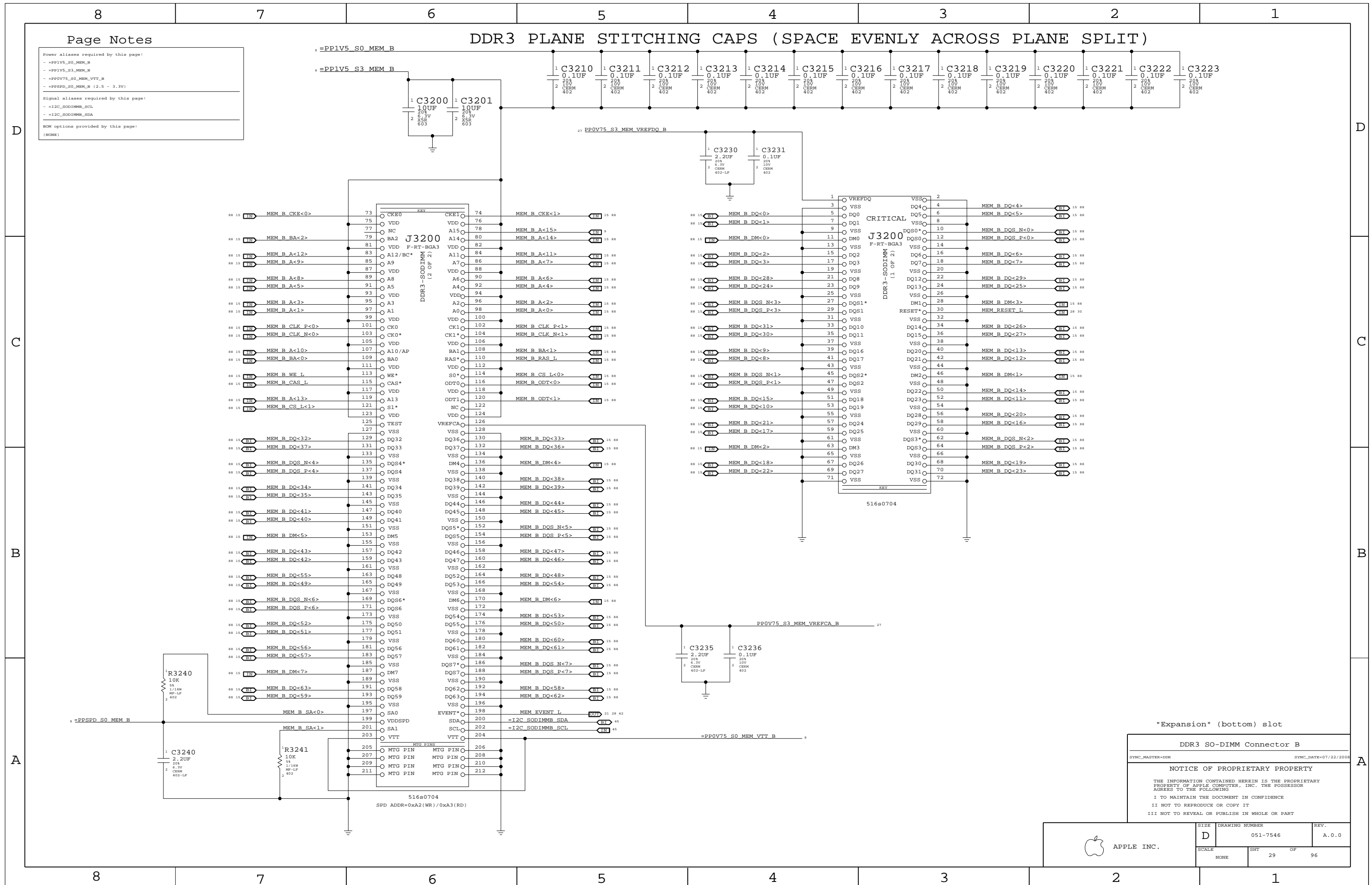
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

"Factory" (top) slot

DDR3 SO-DIMM Connector A		
SYNC_MASTER=DDR	SYNC_DATE=07/22/2008	
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MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



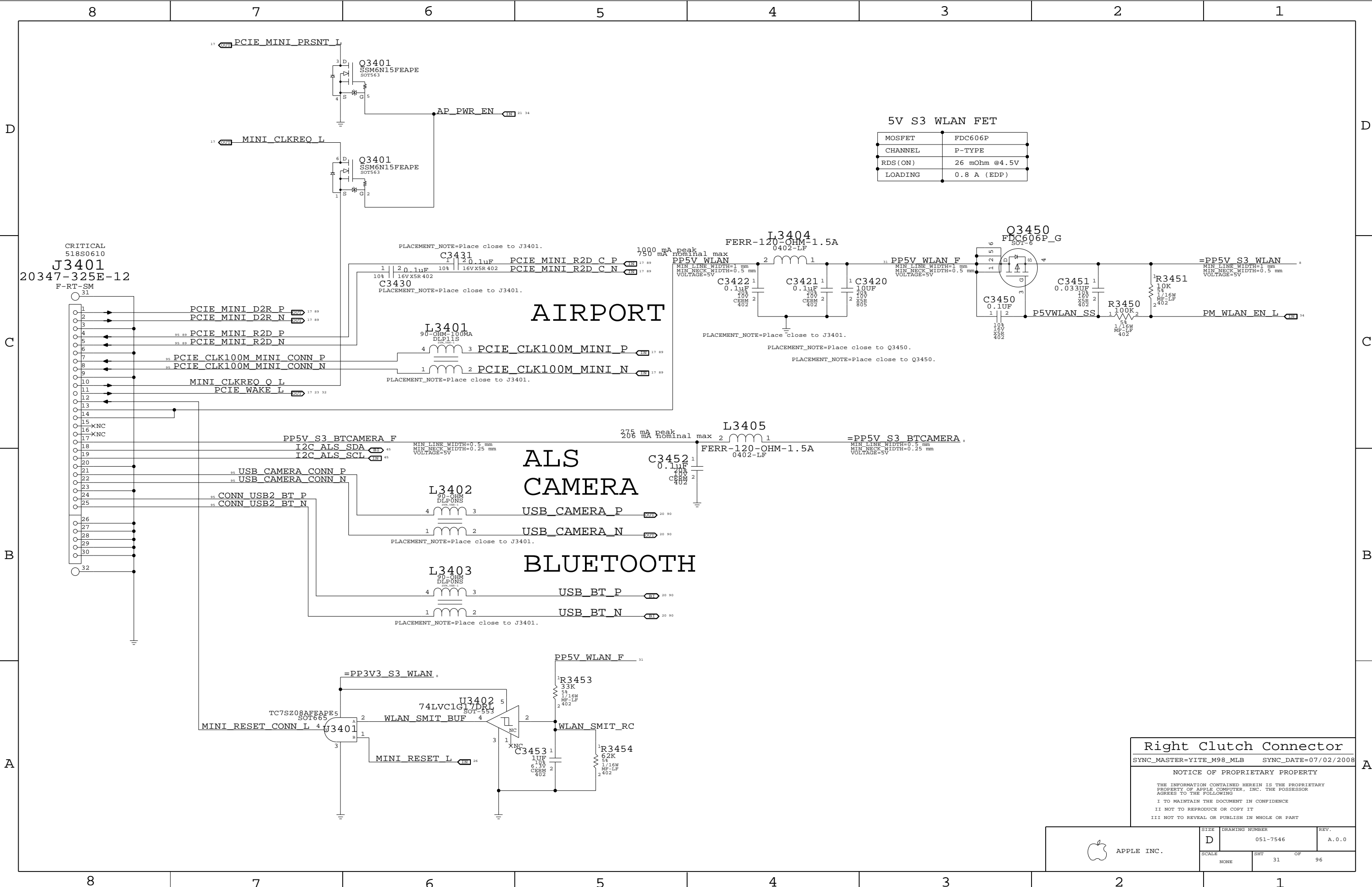
SIZE	
D	

SIZE	DRAWING NUMBER
D	051-7546

V.
A.0.0

SCALE	NONE
-------	------

SHT 30 OF 96



5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Right Clutch Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

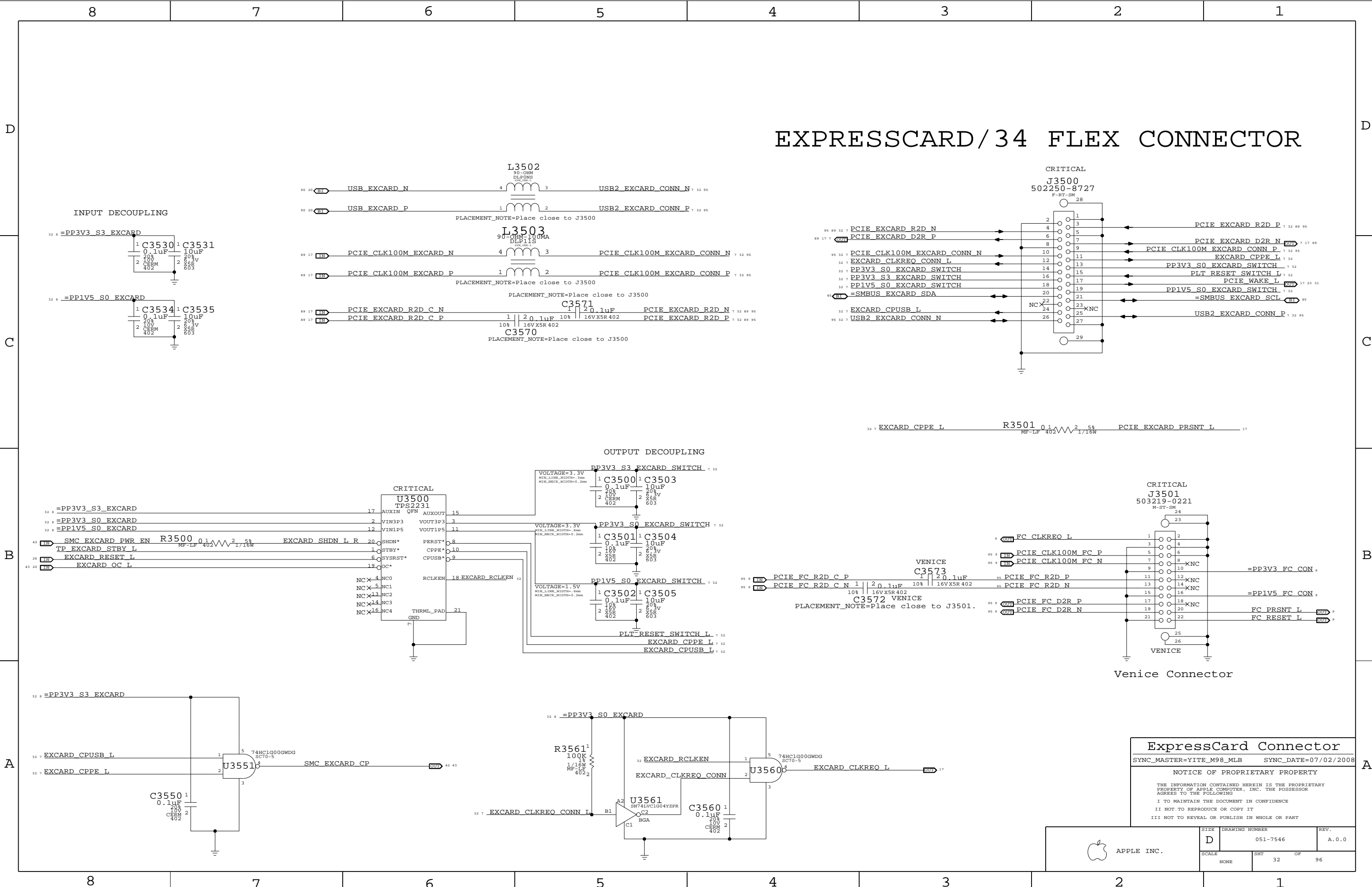
NONE

SHT

31

OF

96



EXPRESSCARD/34 FLEX CONNECTOR

ExpressCard Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	32	96

D

C

B

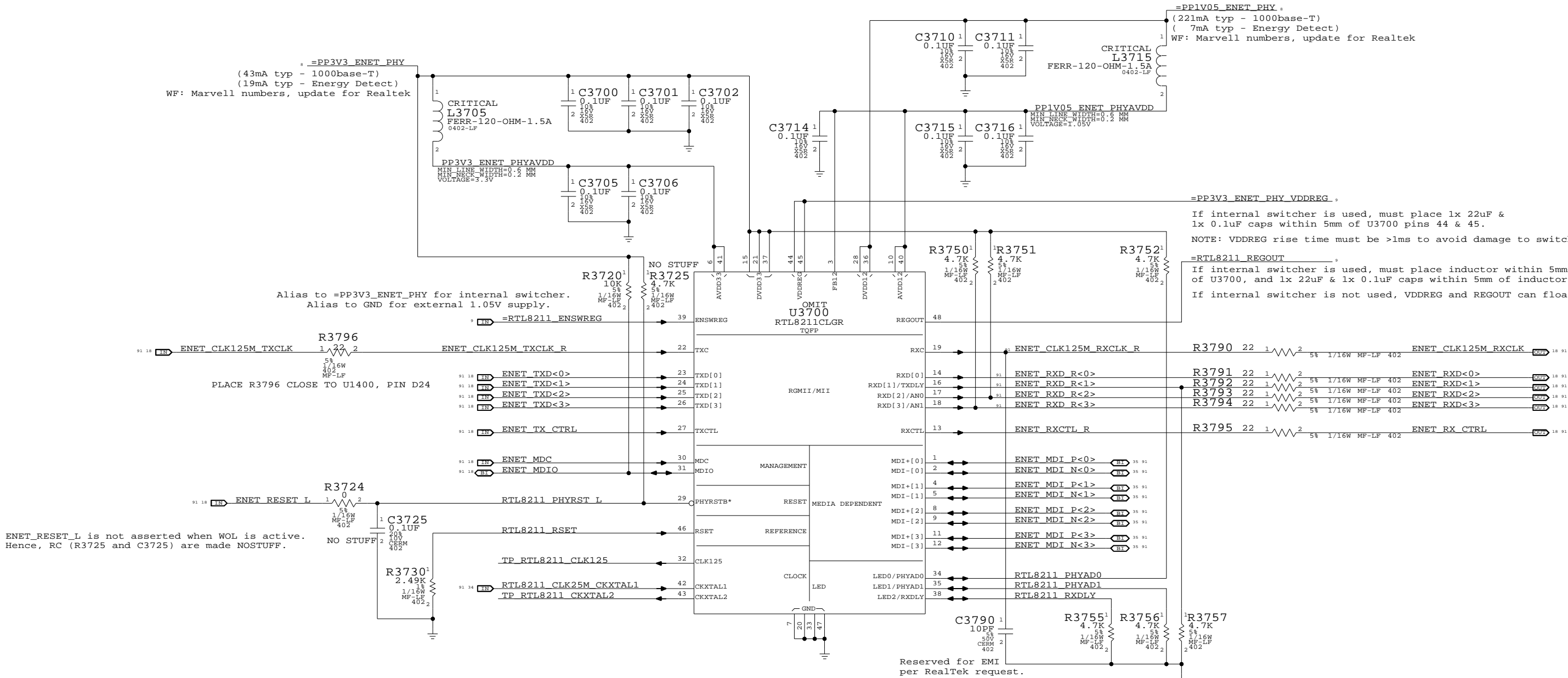
A

D

C

B

A



Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

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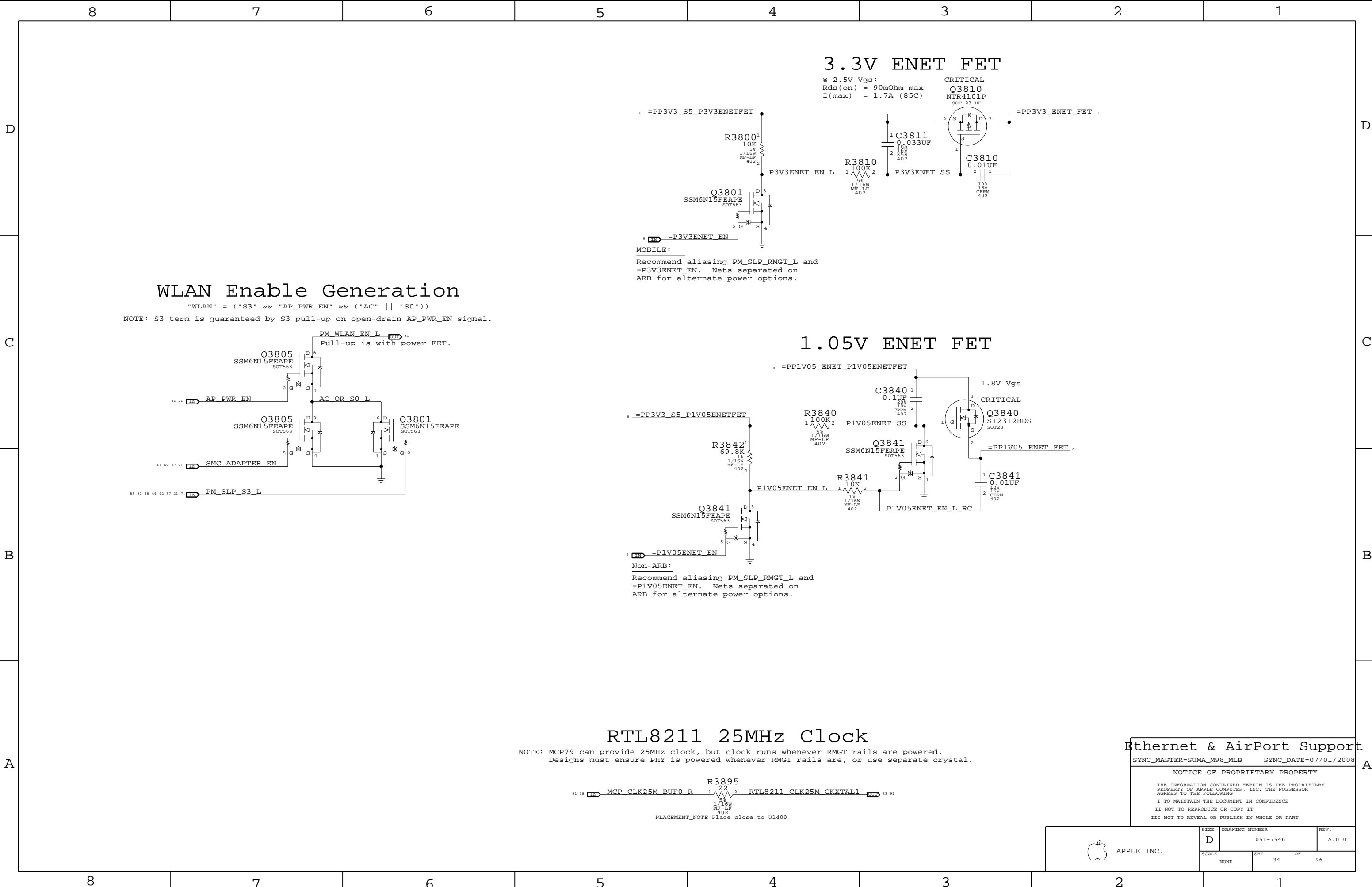
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D	051-7546	A.0.0
SCALE	SHT	OF
NONE	33	96

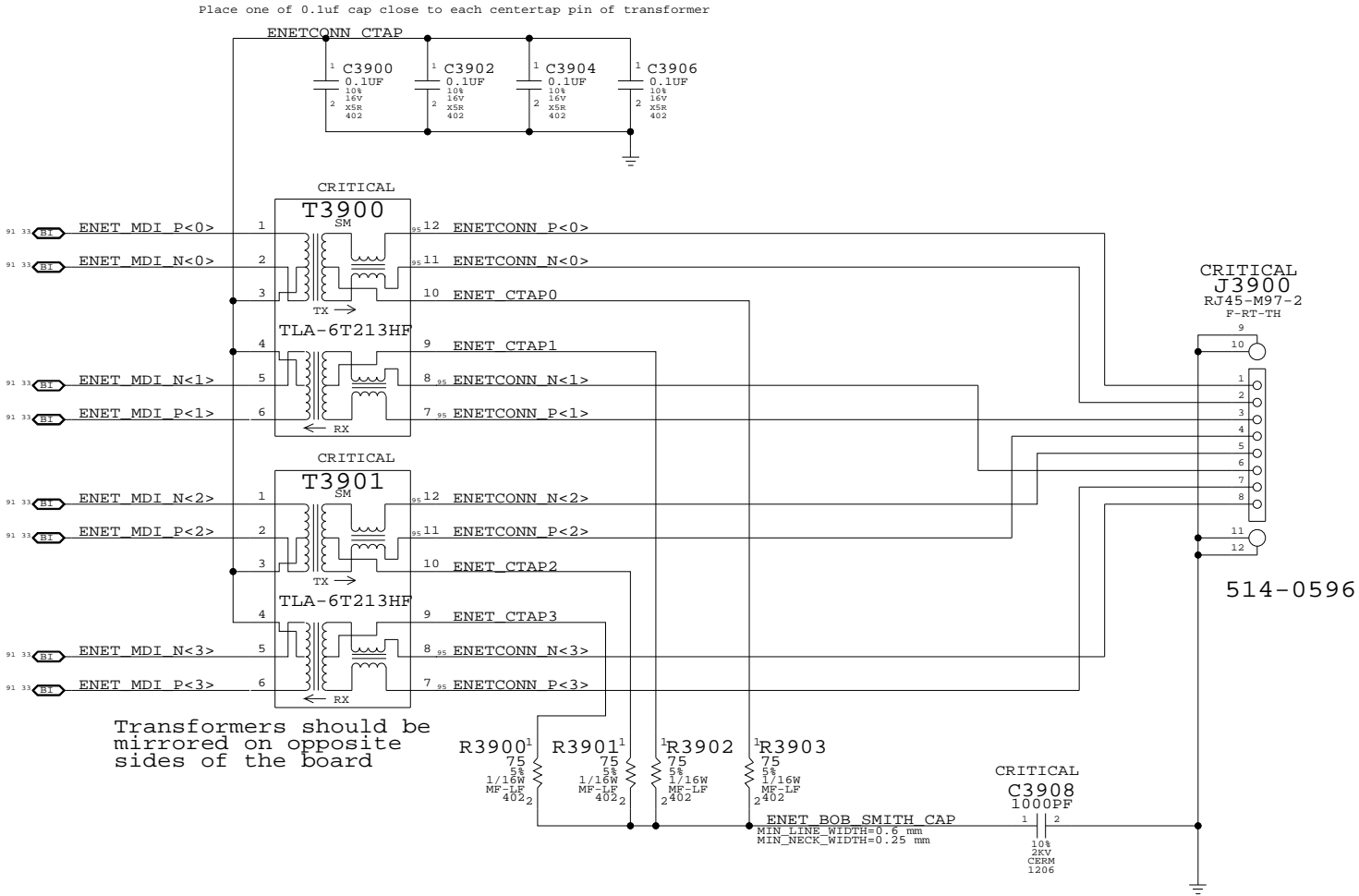


Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

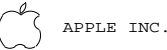
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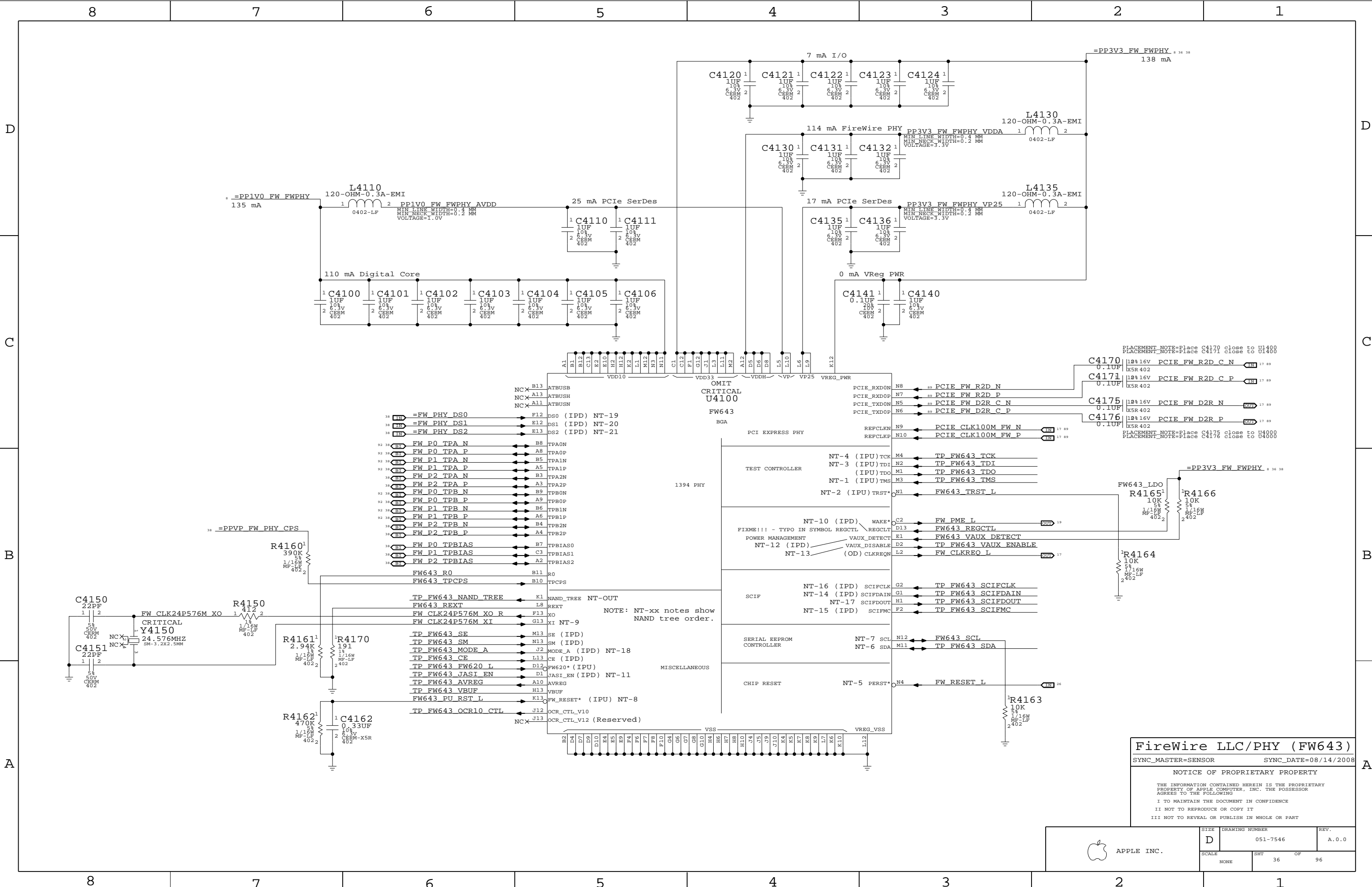
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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	35	96



FireWire LLC/PHY (FW643)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

NONE

SHT

36

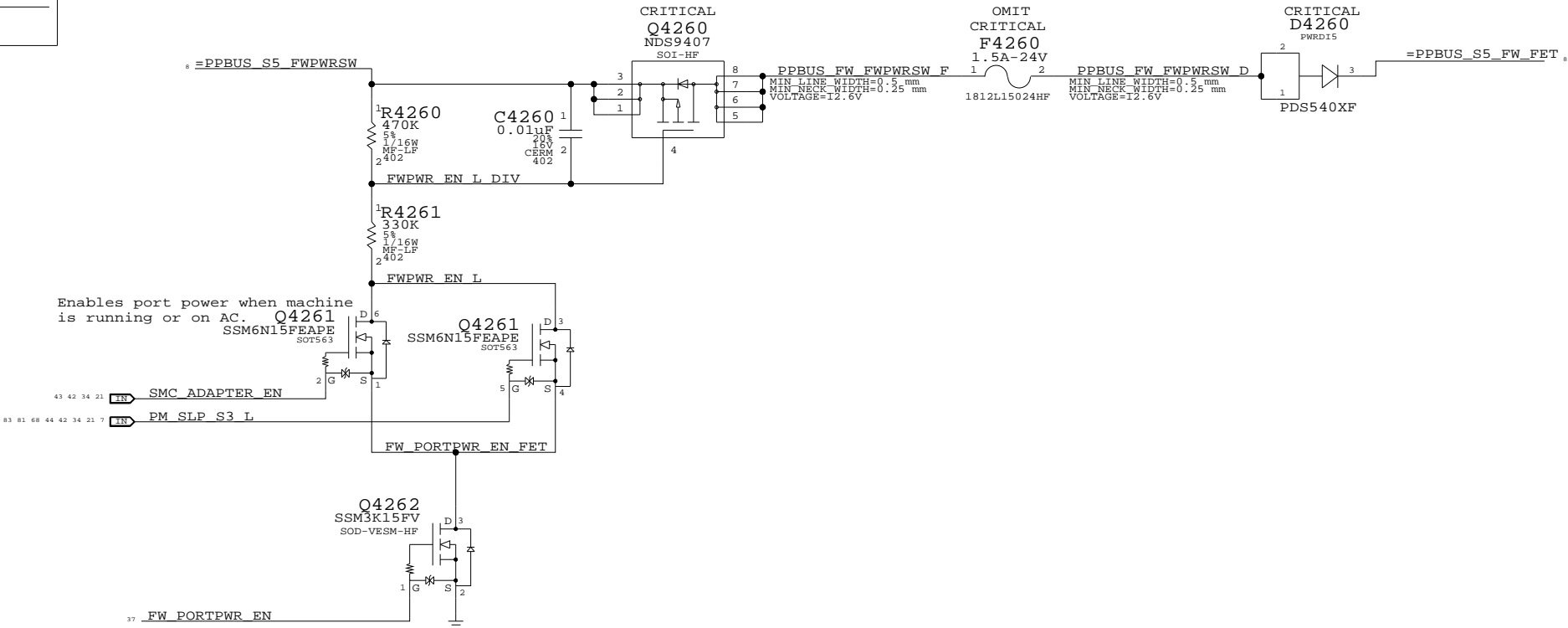
OF

96

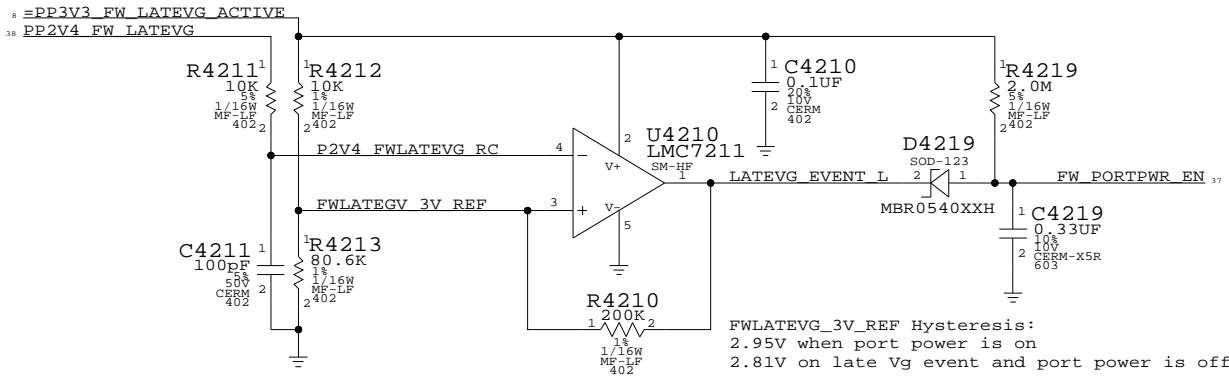
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



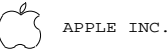
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
740S0080	1	LITTLEFUSE, 1.5A RESETTABLE 24V	F4260	CRITICAL	

FireWire Port Power

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	37	96

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

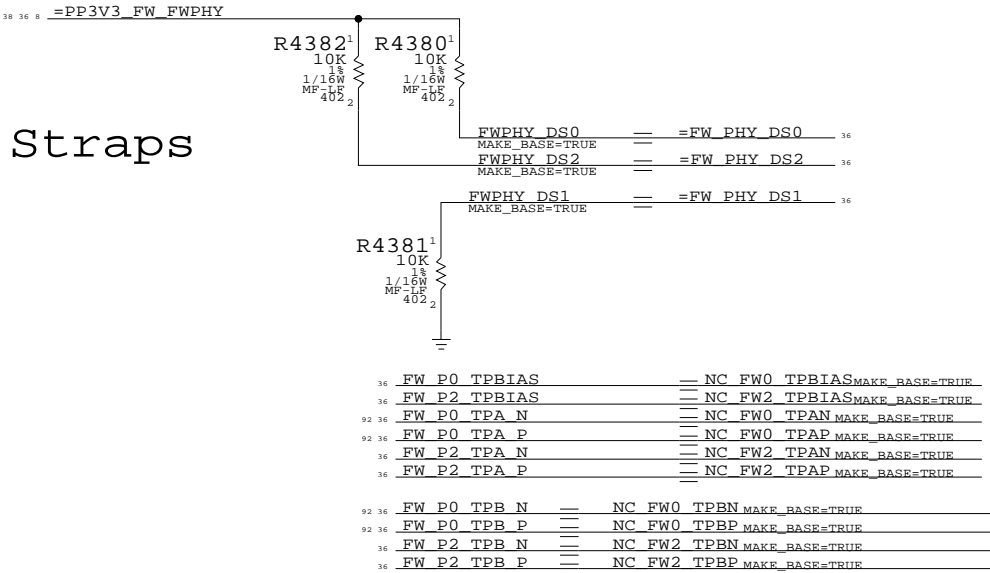
NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

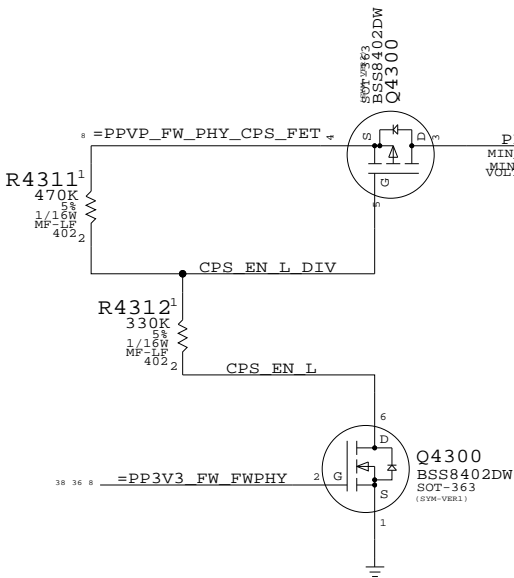
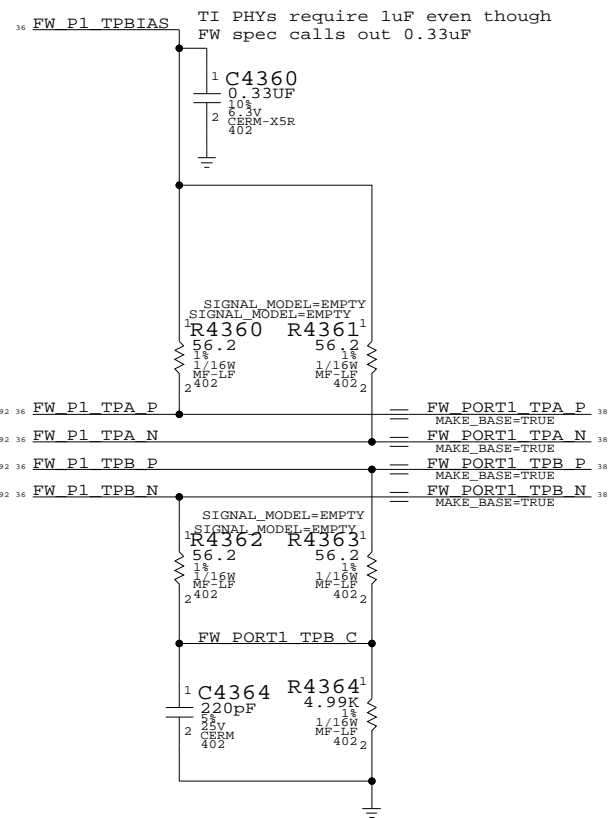
Configures PHY for:

- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

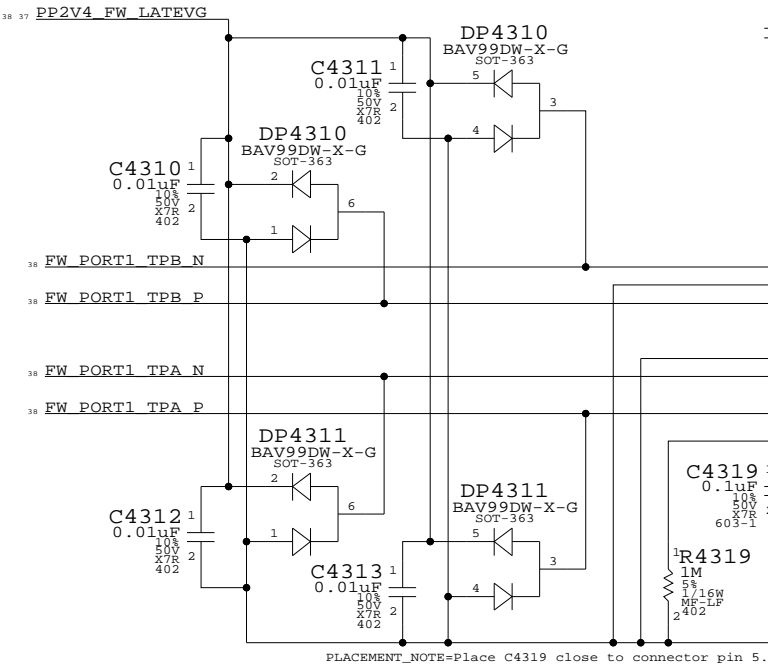


Termination

Place close to FireWire PHY



"Snapback" & "Late VG" Protection

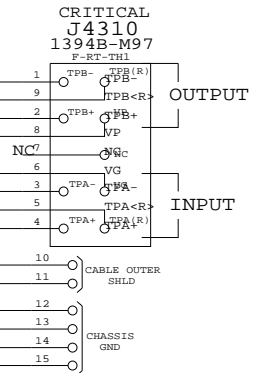


Cable Power

CRITICAL L4310 FERR-250-OHM Note: Trace PPVP_FW_PORT1 must handle up to 5A

Diagram showing Cable Power components. It includes a ferrite bead L4310 (FERR-250-OHM) and a capacitor C4314 (0.01uF). The diagram shows the connection of PPVP_FW_PORT1 to the ferrite bead and capacitor.

PORT 1 BILINGUAL

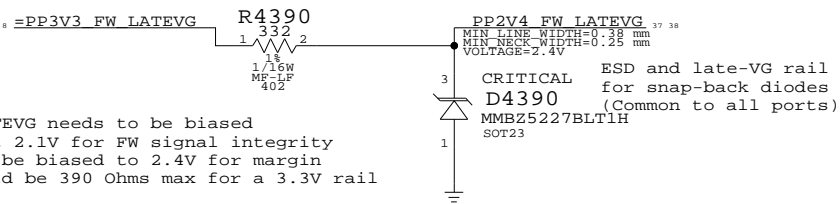


AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power



PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin

R4390 should be 390 Ohms max for a 3.3V rail

FireWire Ports

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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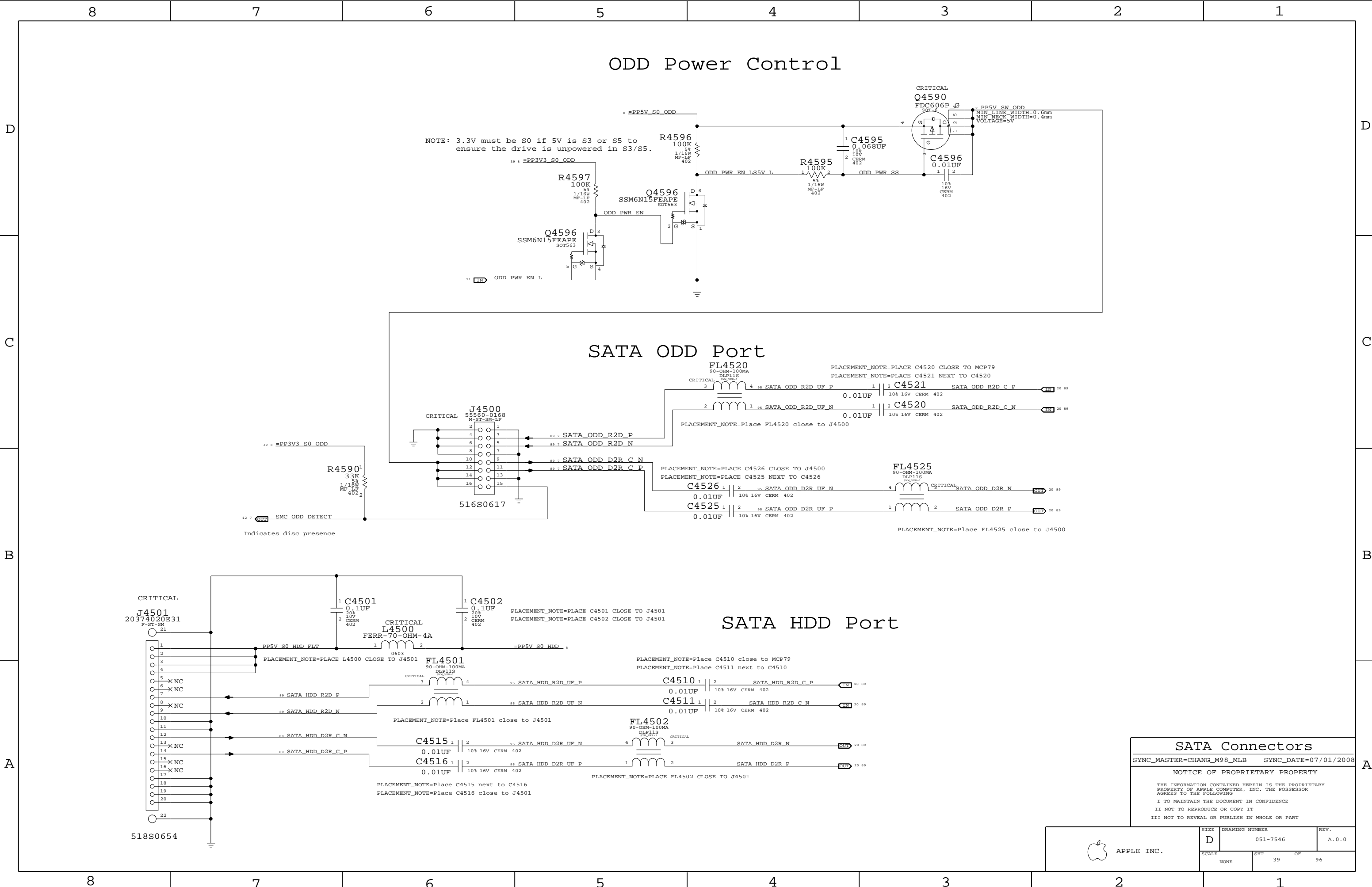
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NONE	38	96



ODD Power Control

SATA ODD Port

SATA HDD Port

SATA Connectors

SYNC_MASTER=CHANG_M98_MLB

SYNC_DATE=07/01/2008

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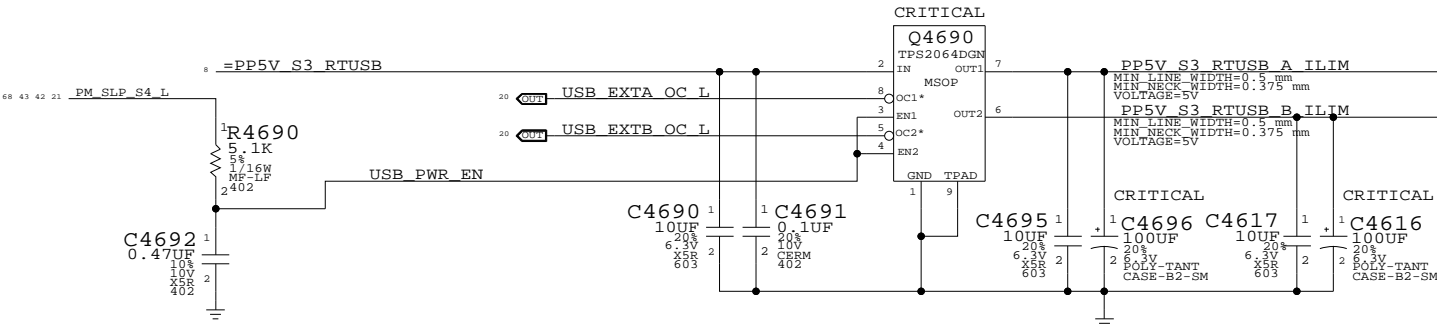
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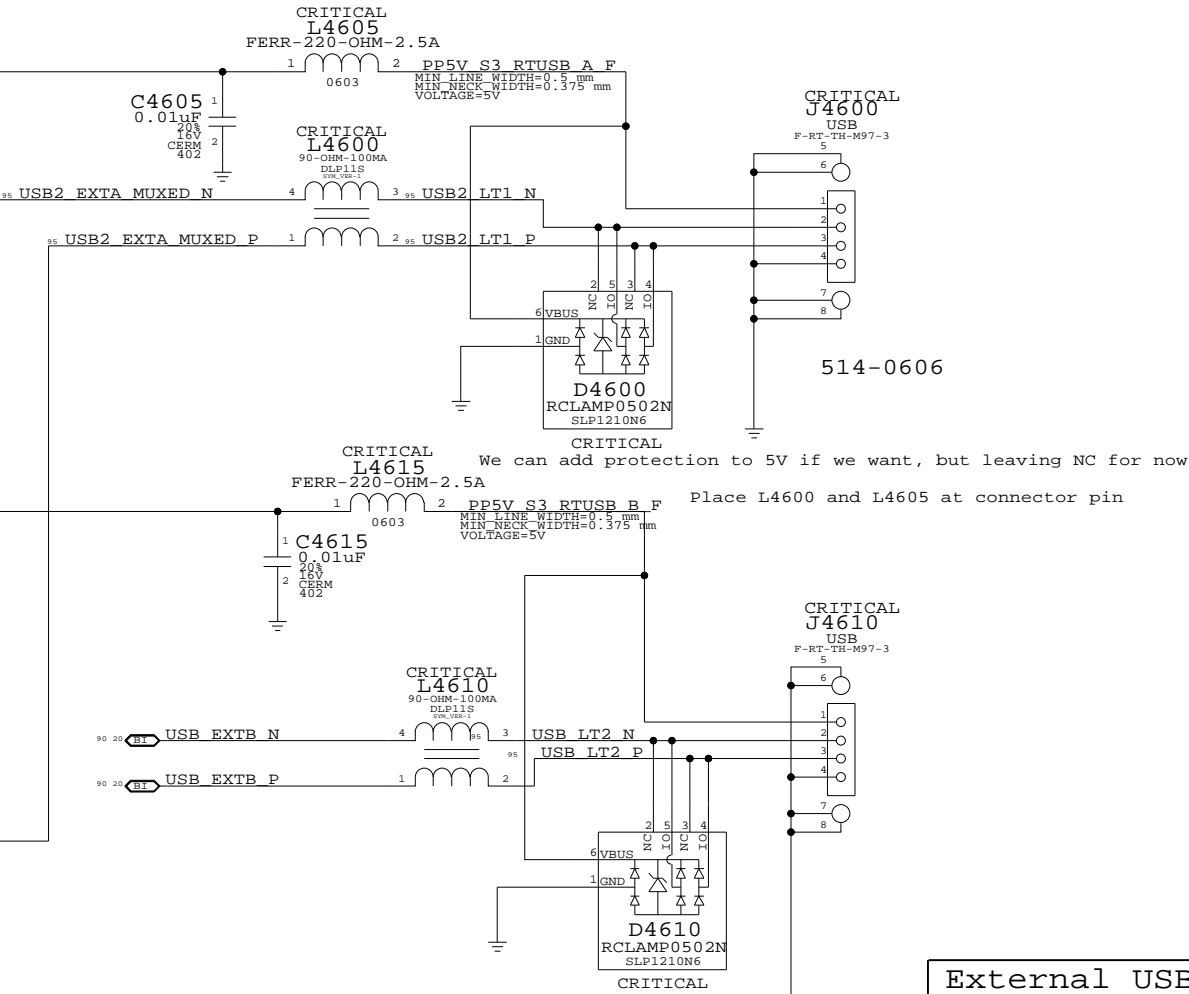
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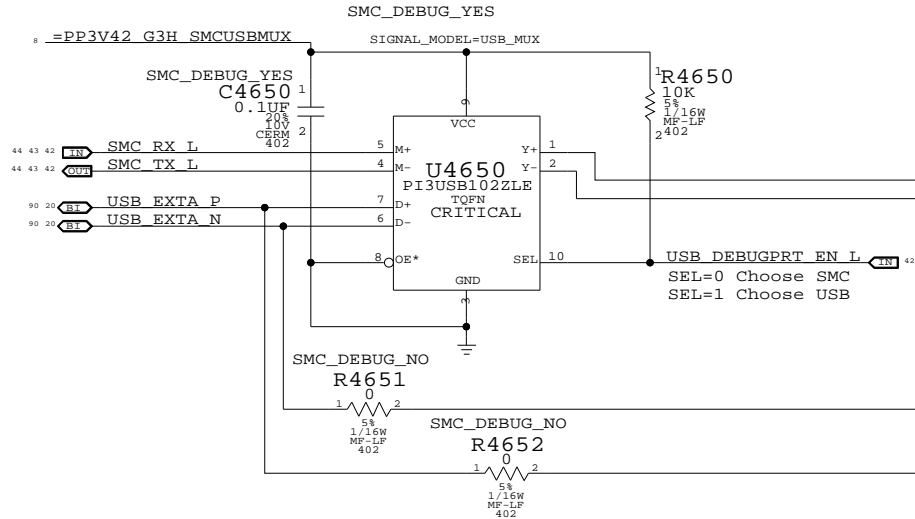
Port Power Switch



Left USB Port A



USB/SMC Debug Mux



Left USB Port B

External USB Connectors

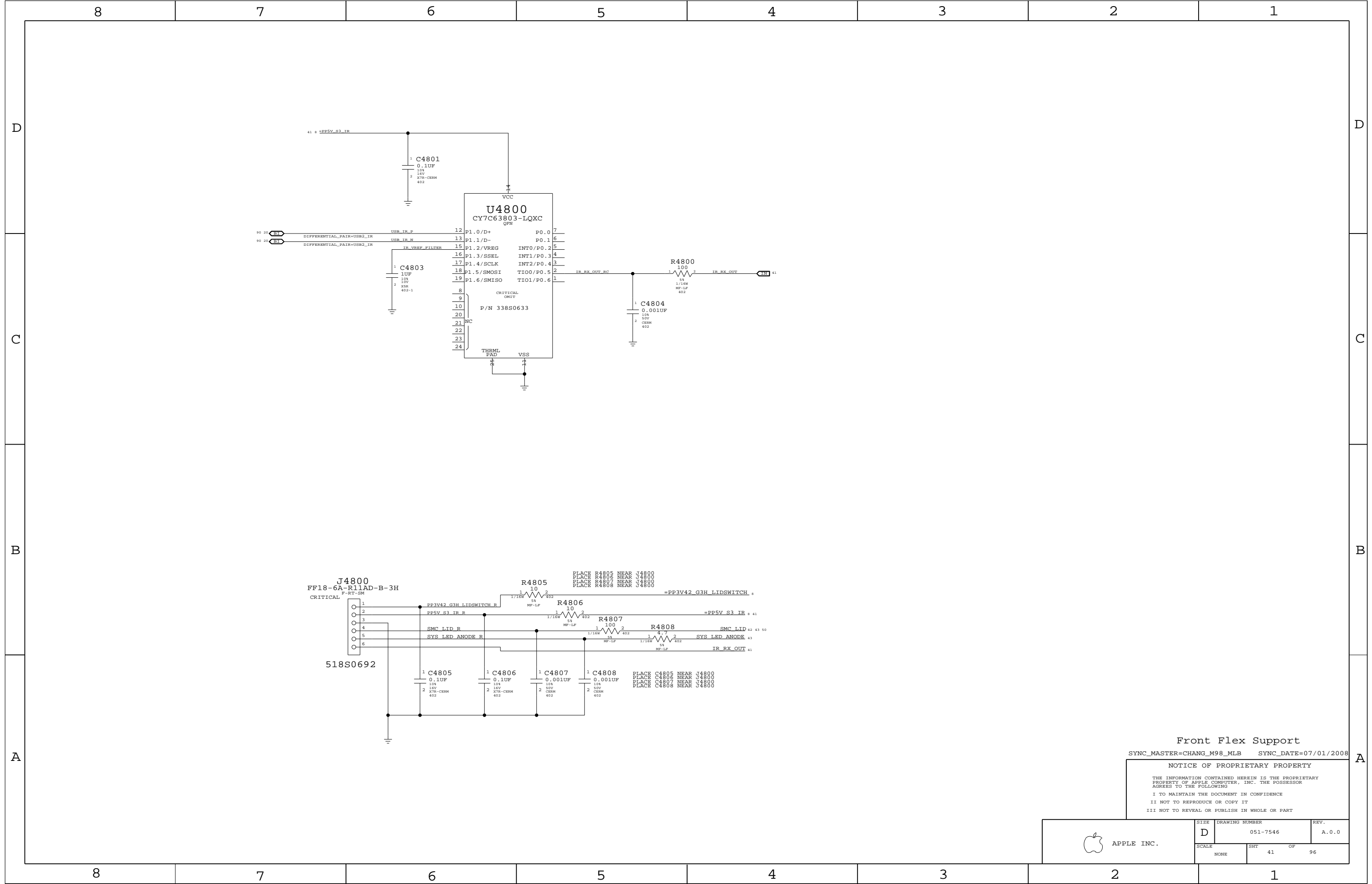
SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008

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SCALE	SHT	OF
NONE	40	96



Front Flex Support

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

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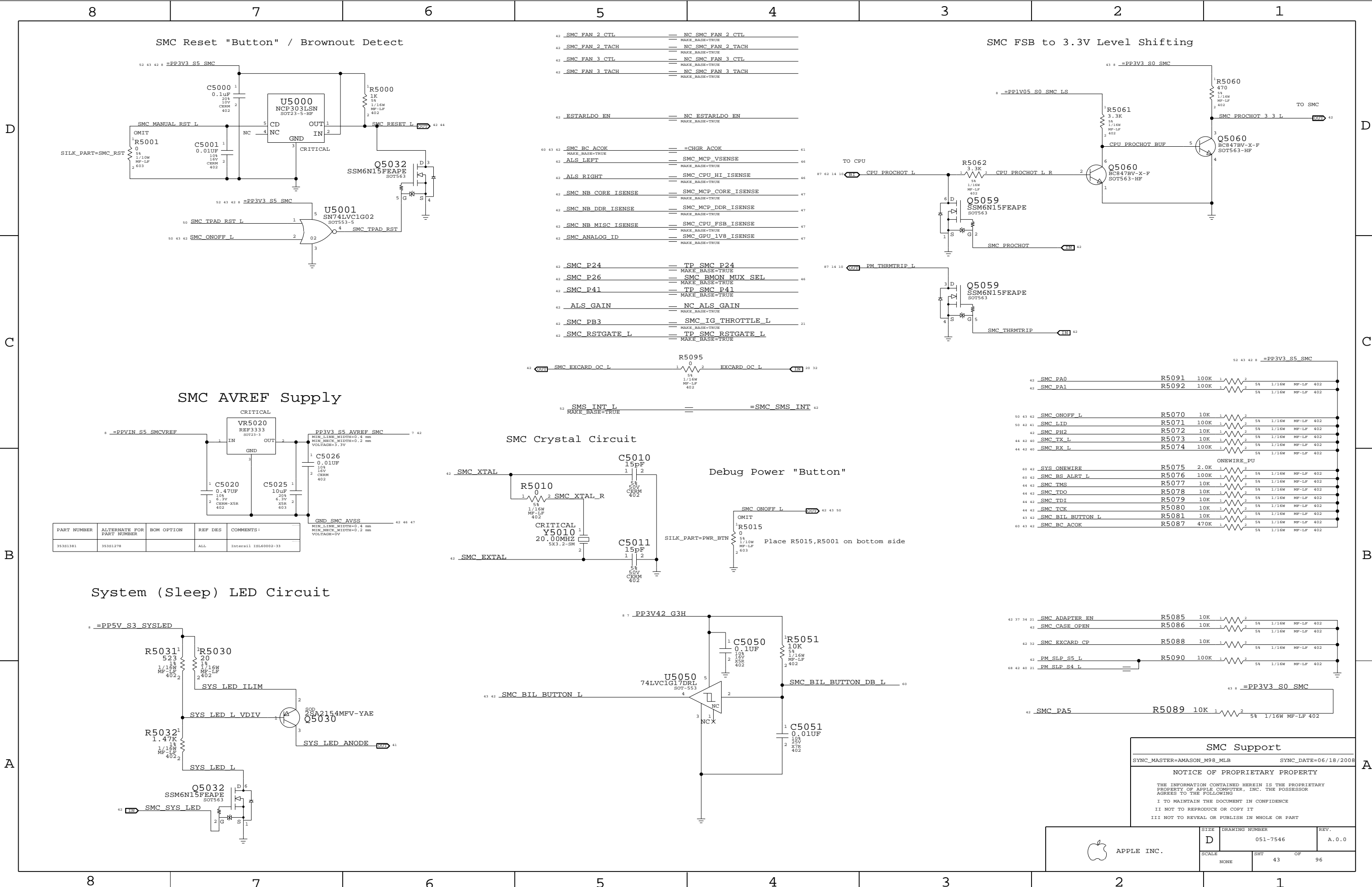
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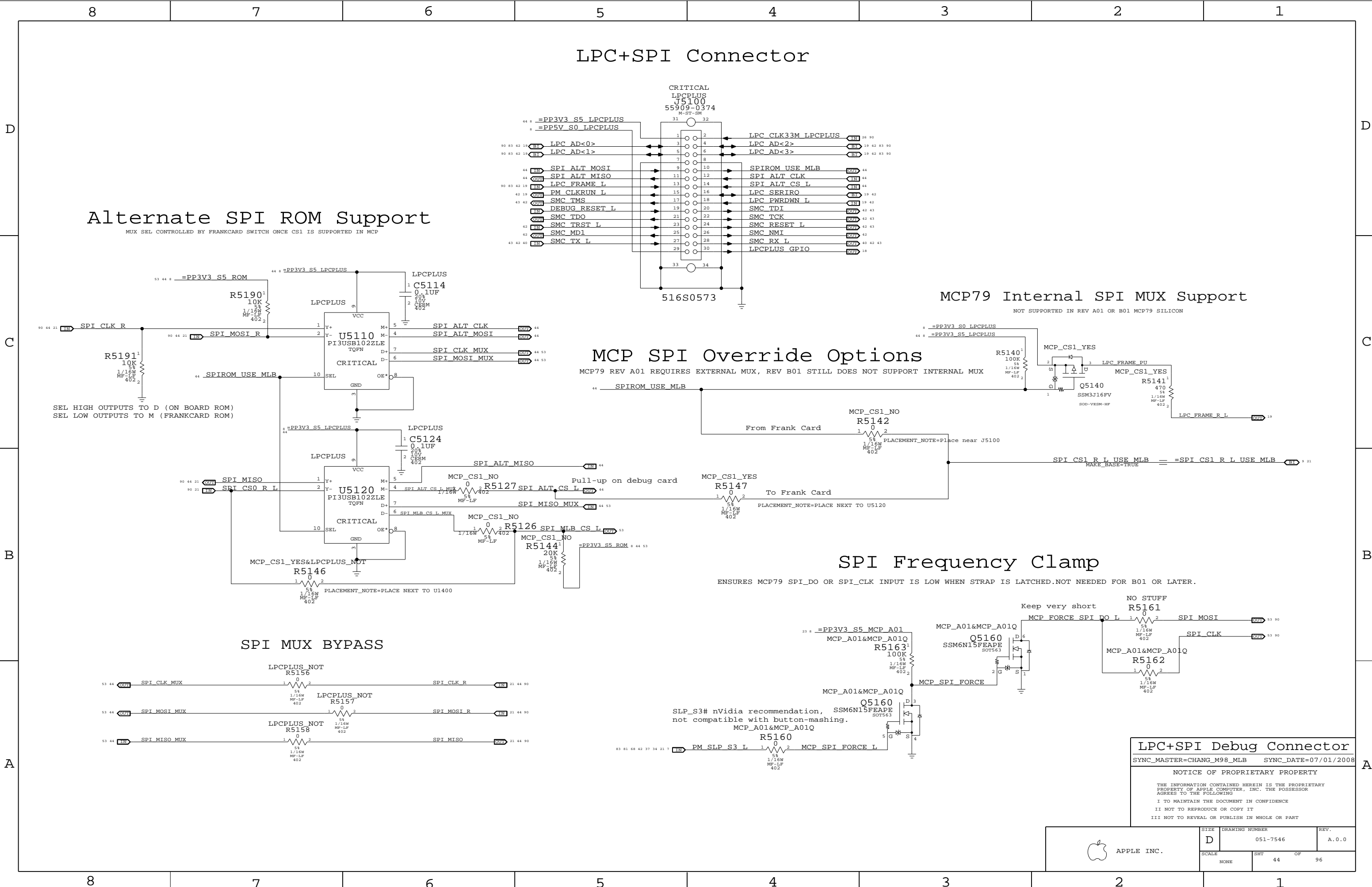
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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	41	96





LPC+SPI Connector

Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED. NOT NEEDED FOR B01 OR LATER.

SPI MUX BYPASS

LPC+SPI Debug Connector

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

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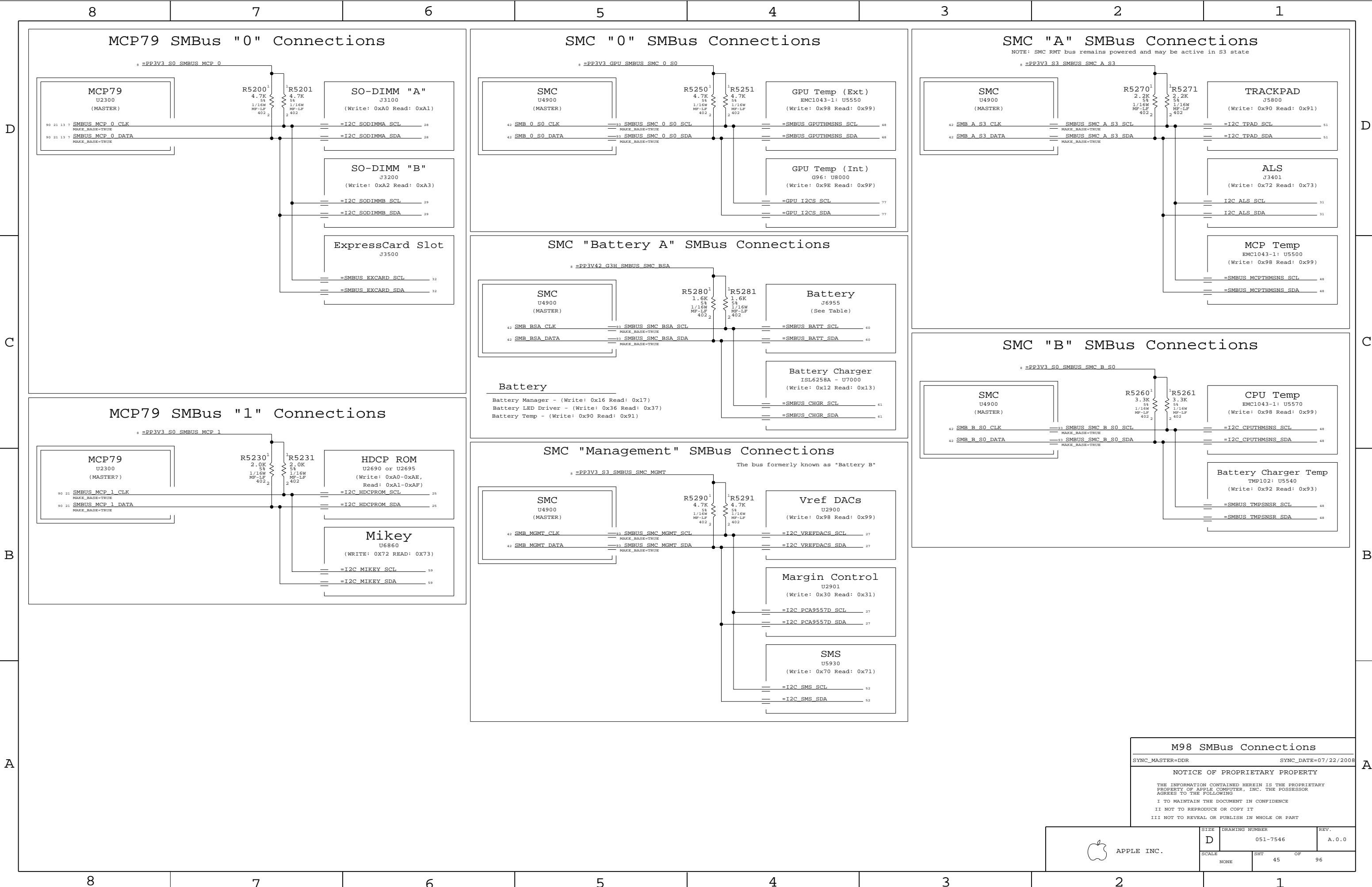
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APPLE INC.

SIZE D DRAWING NUMBER 051-7546 REV. A.0.0

SCALE NONE SHT 44 OF 96



M98 SMBus Connections

SYNC_MASTER=DDR

SYNC_DATE=07/22/2008


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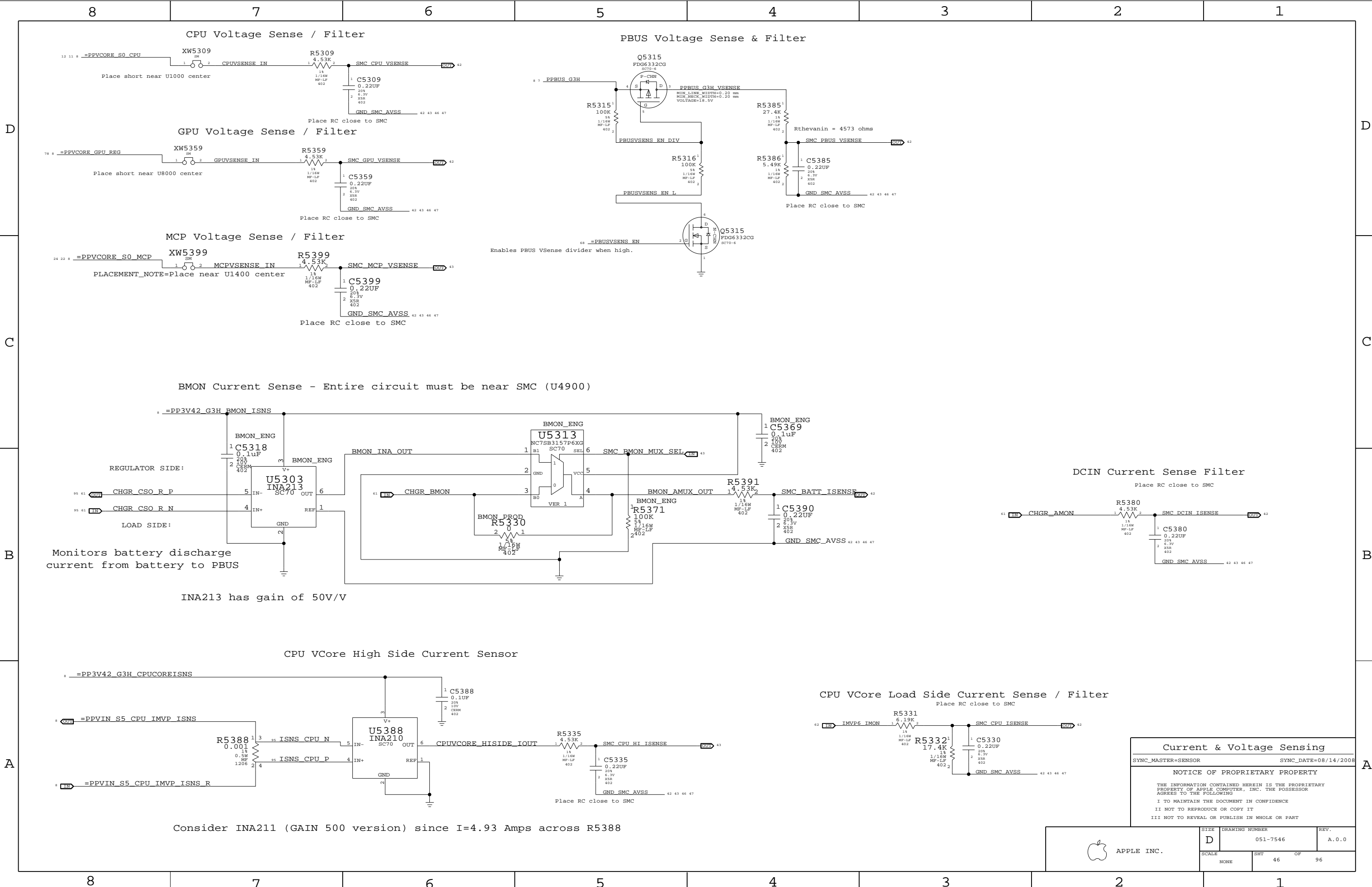
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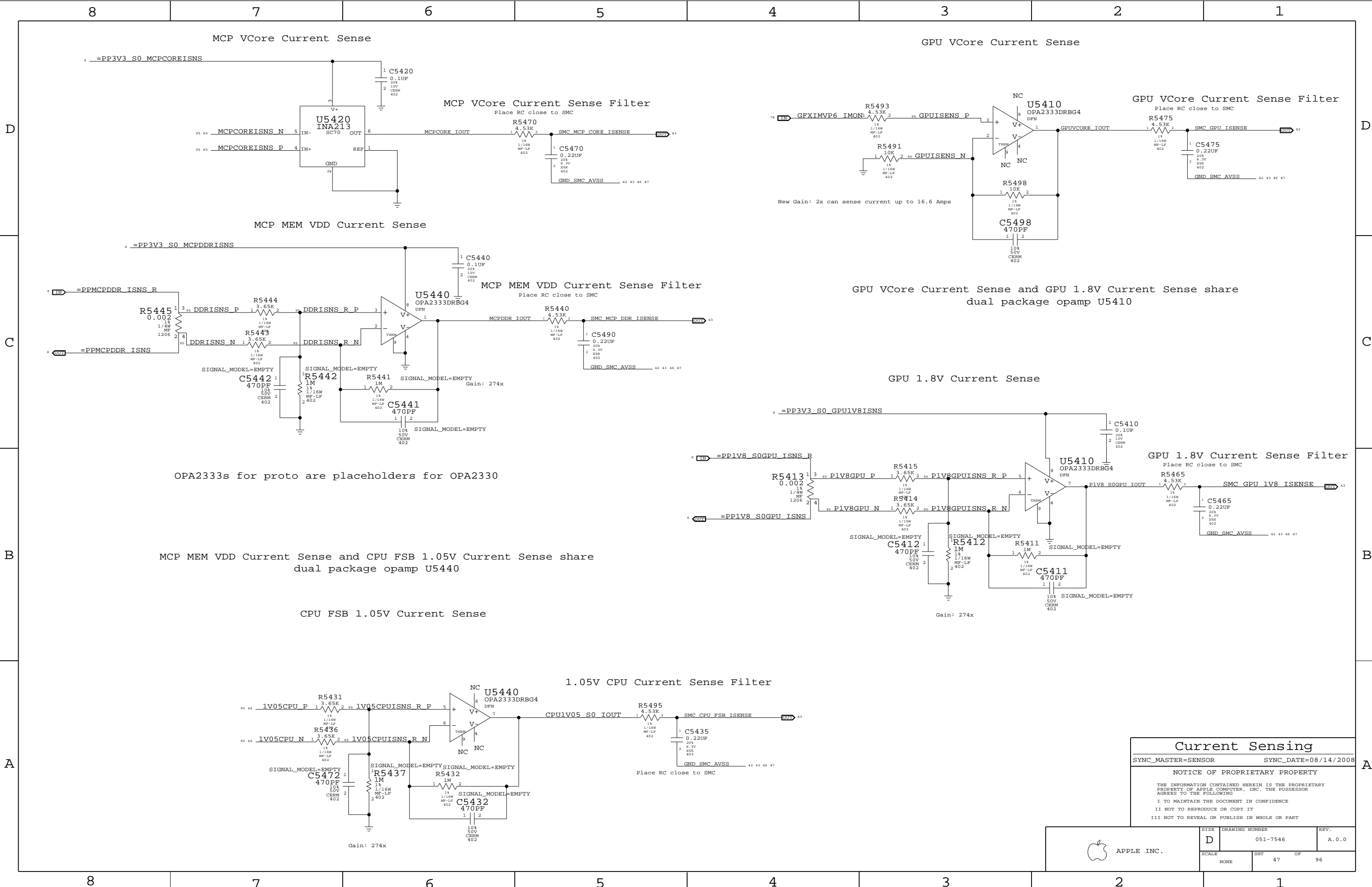
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	SCALE NONE	SHT 45	OF 96





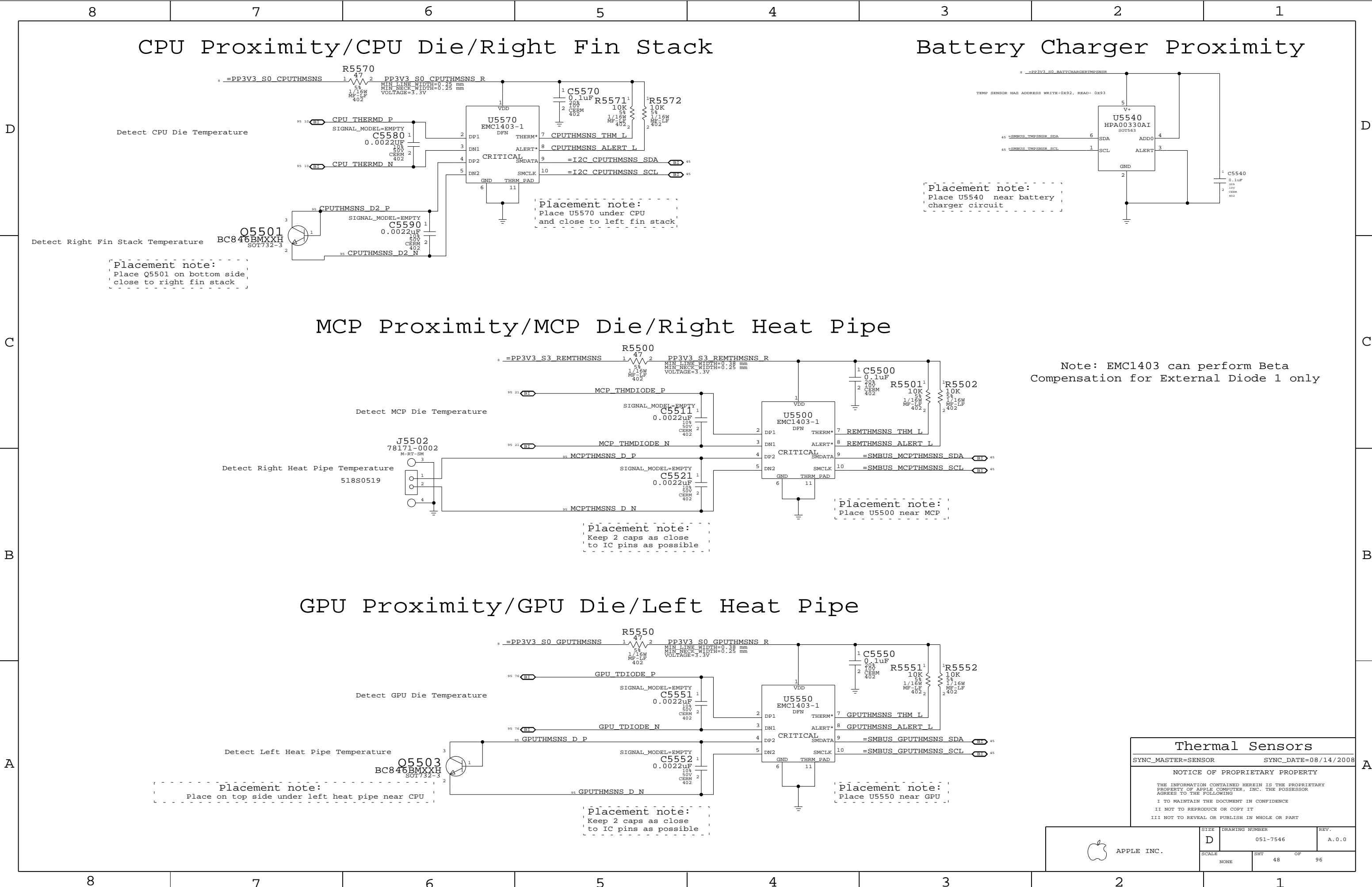
OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

Current Sensing		
SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
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SCALE		SHT	OF
NONE		47	96



CPU Proximity/CPU Die/Right Fin Stack

Battery Charger Proximity

MCP Proximity/MCP Die/Right Heat Pipe

GPU Proximity/GPU Die/Left Heat Pipe

Note: EMC1403 can perform Beta Compensation for External Diode 1 only

Thermal Sensors

SYNC_MASTER=SENSOR

SYNC_DATE=08/14/2008


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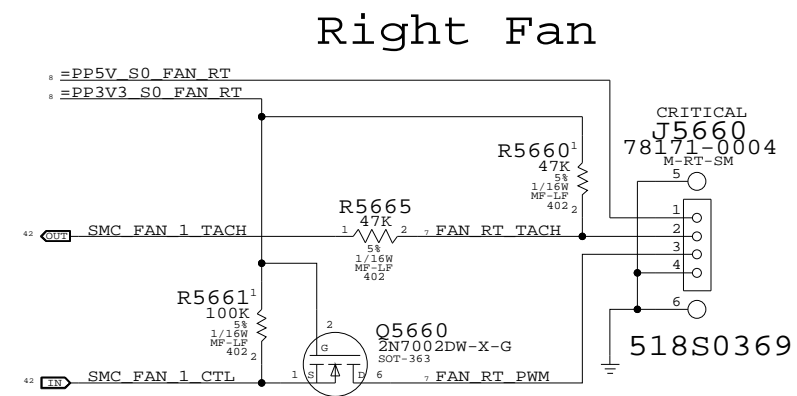
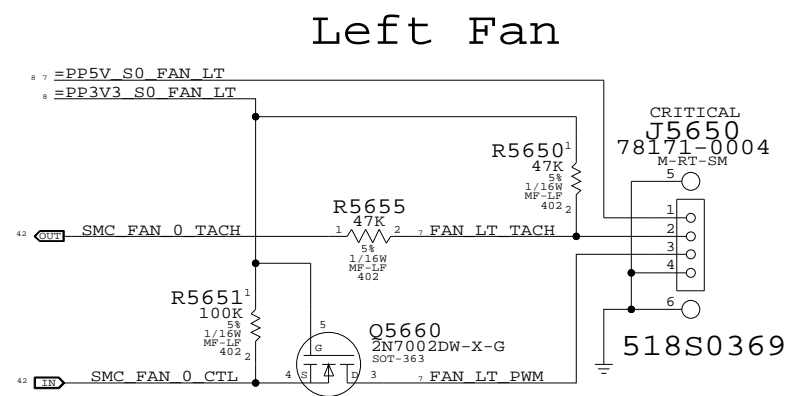
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 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7546		A.0.0
SCALE		SHT	OF	96
NONE		48		



Fan Connectors

SYNC_MASTER=M87_MLB	SYNC_DATE=10/17/2007	7
---------------------	----------------------	---

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APPLE INC.

SIZE
D

SIZE	DRAWING NUMBER
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D	051-7546
---	----------

4.0.0

SCALE	

NON

SHT	
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49

OF	
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96

8

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D

C

C

B

B

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A

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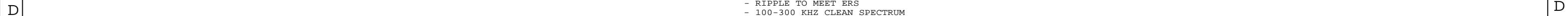
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3

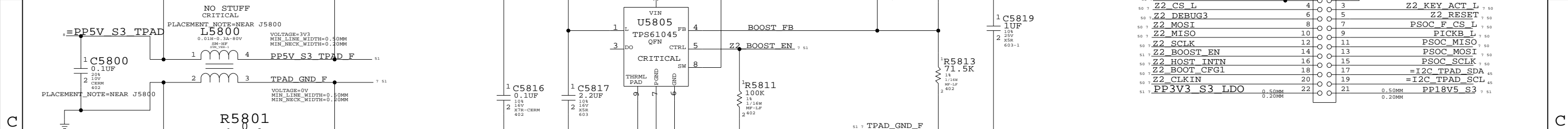
2

1

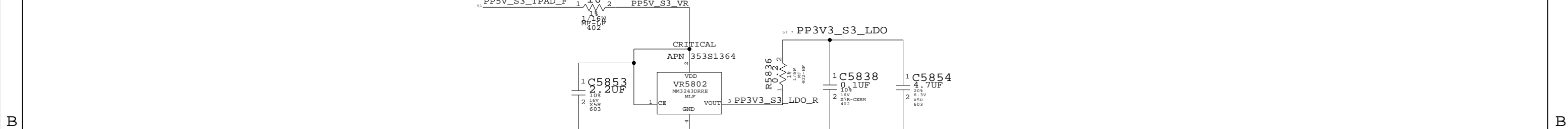
8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



<p>PP5V_S3_TPAD_F</p> <p>APN 15280504</p> <p>CRITICAL</p> <p>75301</p>	<p>- R5812,R5813,C5818 MODIFIED</p>	<p>IPD FLEX CONNECTOR</p>
--	-------------------------------------	---------------------------



3V3 LDO FOR IPD



Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

1098AS-SM

FF18-4A-R11AD-B-3H

J5815

SMC_KBDLED_PRESENT_L

SMC_SYS_KBDLED

R5853

C5850

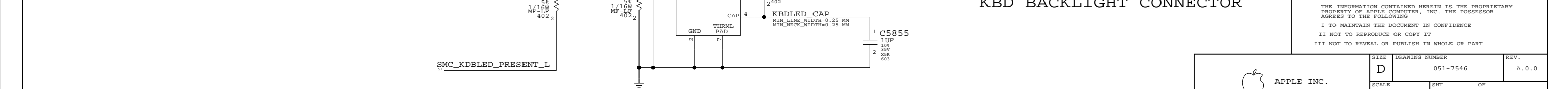
LED

KBDLED_SW

KBDLED_ANODE

WELLSPRING 2

A	R5853 ALWAYS PRESENT	R5854 ¹	R5852 ¹	LT3491	10 15 16W	LINE-MASTER-PROGRAM- LINE-DATE 09/12/2008	A
				DFN		NOTICE OF PROPRIETARY PROPERTY	



RS833 ADWAS PRESENT RS833 ADWAS PRESENT 4-7K \times 14129 \times	RS833 ADWAS PRESENT 10K \times 14129 \times	DPN 1/16W 2402 \times
---	---	-------------------------------

KBD BACKLIGHT CONNECTOR

NOTICE OF PROPRIETARY PROPERTY
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BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT

NO STUFF

R5852¹

R5854¹

4.7K

10K

1/16W

1/16W

402

402

CRITICAL

U5850

LT3491

DFN

LED

5

4

KBDLED ANODE

MIN_LINE_WIDTH=0.25 MM

MIN_NECK_WIDTH=0.25 MM

APN 518S0612

KBDLED_CAP

MIN_LINE_WIDTH=0.25 MM

MIN_NECK_WIDTH=0.25 MM

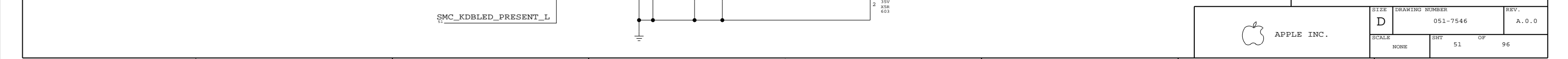
C5855

1UF

108

KBD BACKLIGHT CONNECTOR

WELLSPRING 2	
SYNC_MASTER=PWRSQNC	SYNC_DATE=05/12/2008
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[illegible]

SCALE	SHT	OF
XXXX	51	96

1	2	3	4	5	6	7	8
1	2	3	4	5	6	7	8

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

D

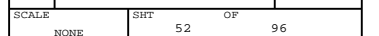


D



B

A



D

C

B

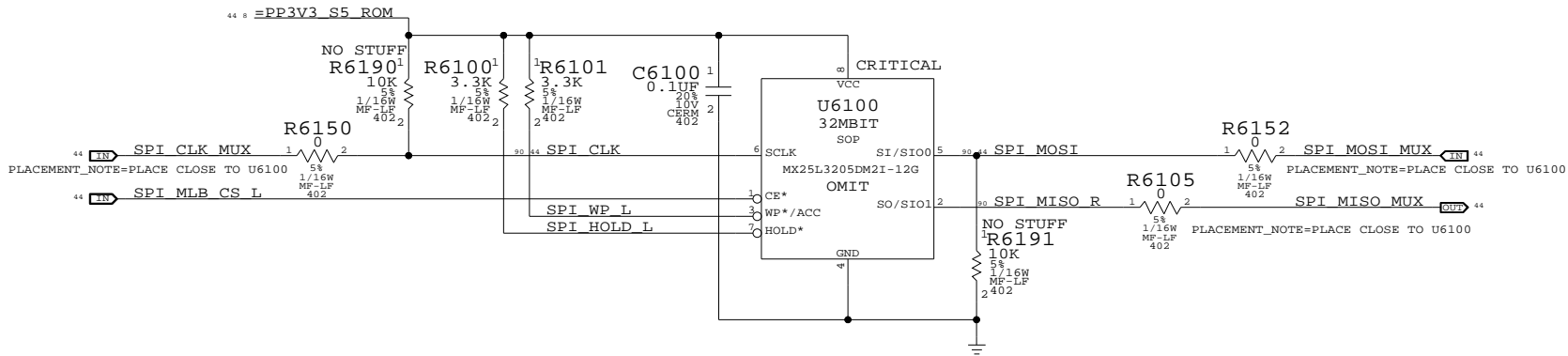
A

D

C

B

A



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

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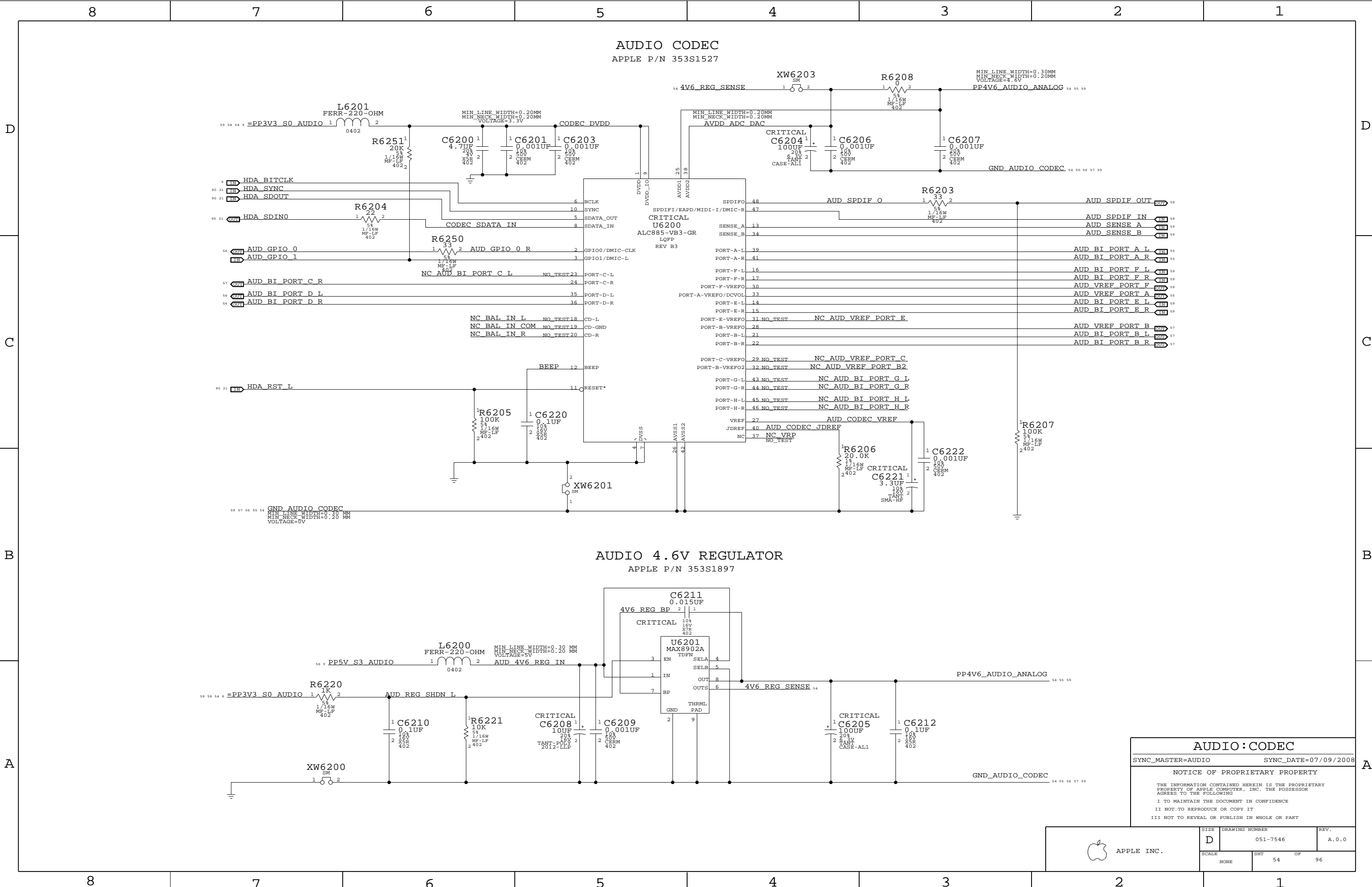
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SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
SCALE NONE	SHT 53 OF 96	



AUDIO:CODEC

SYNC_MASTER=AUDIO

SYNC_DATE=07/09/2008


NOTICE OF PROPRIETARY PROPERTY

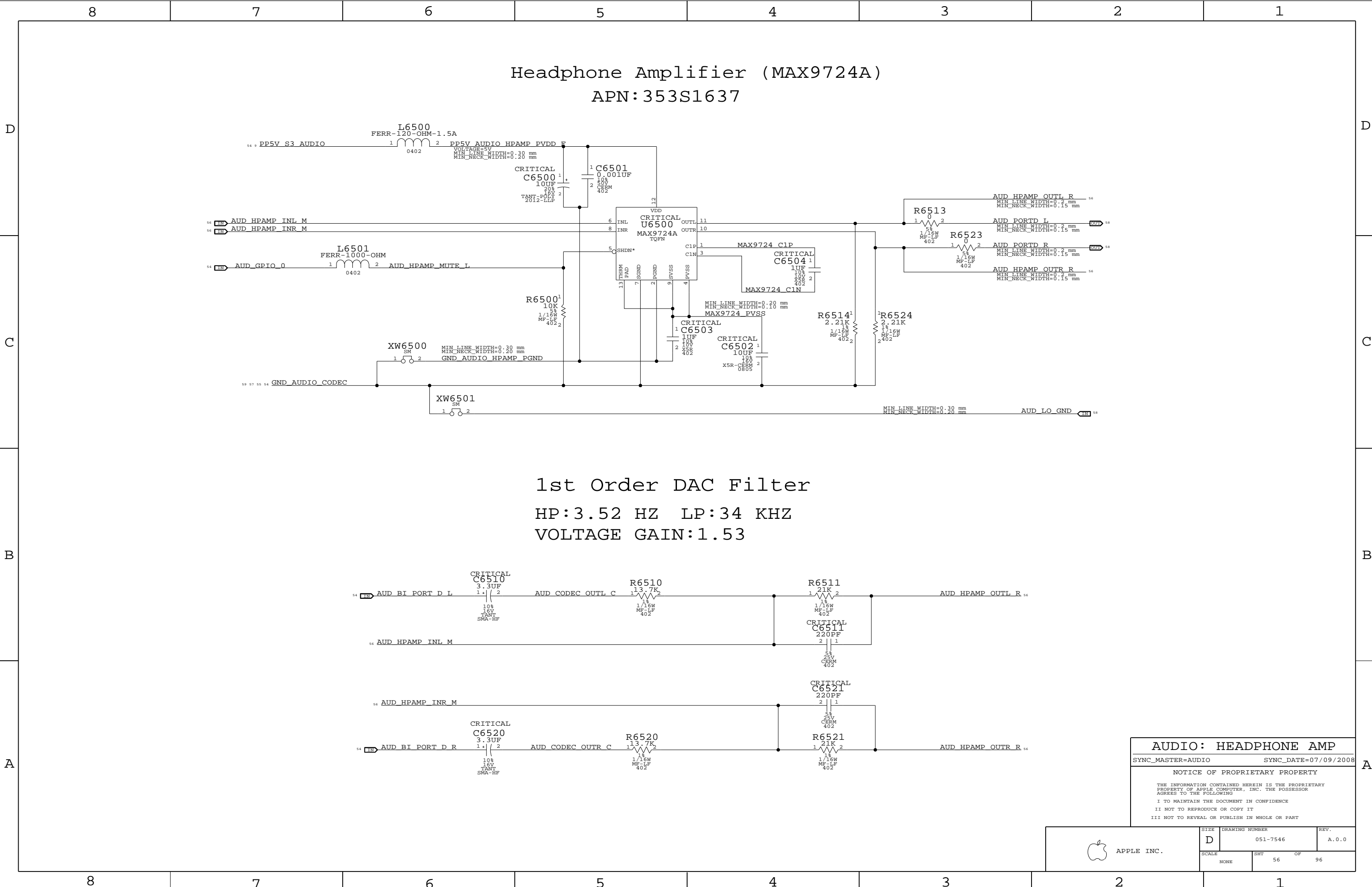
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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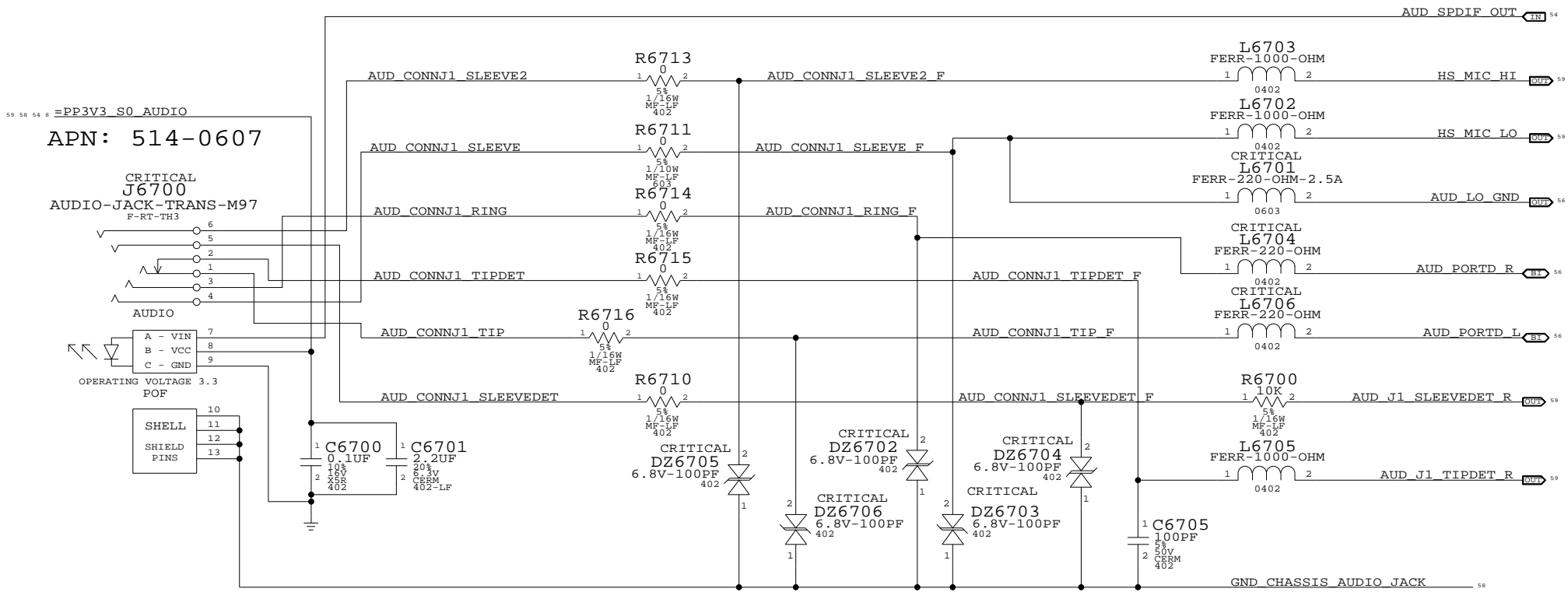
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

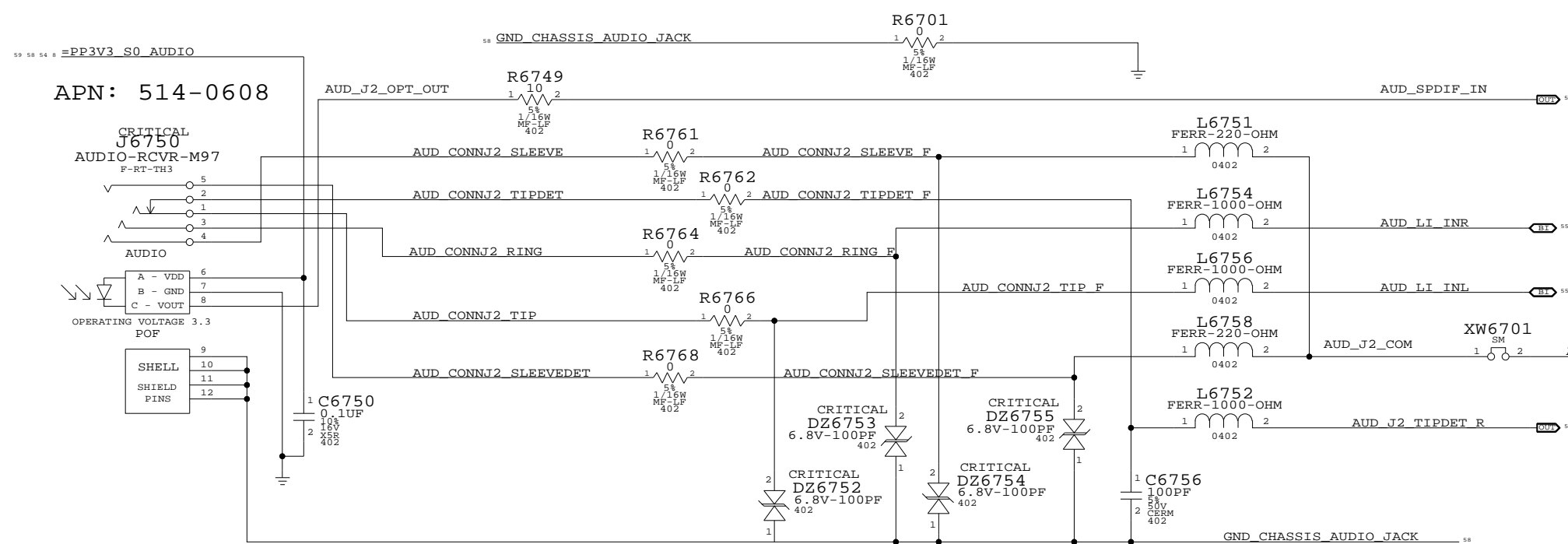
 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7546		A.0.0
SCALE		NONE	SHT	OF
			54	96



AUDIO JACK 1 LO/HP JACK, SPDIF TX



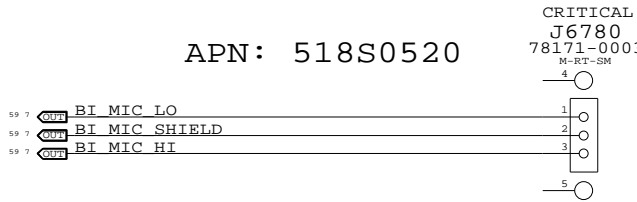
RETURN FOR HF NOISE



AUDIO JACK 2 LINE IN JACK, SPDIF RX

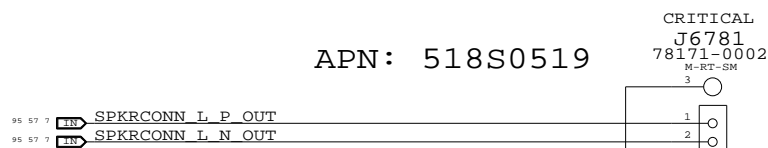
MIC CONNECTOR

APN: 518S0520

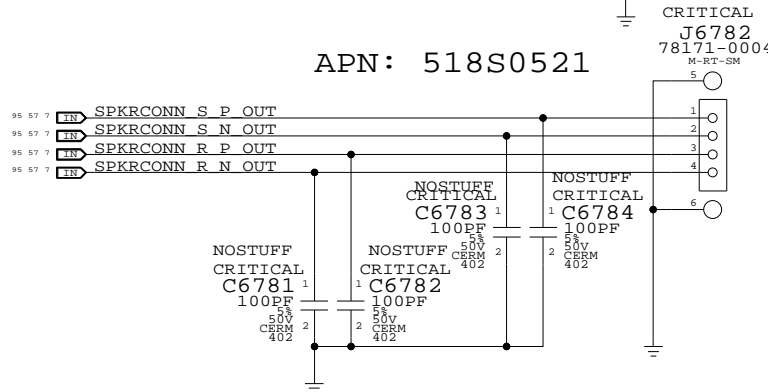


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



AUDIO: JACKS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

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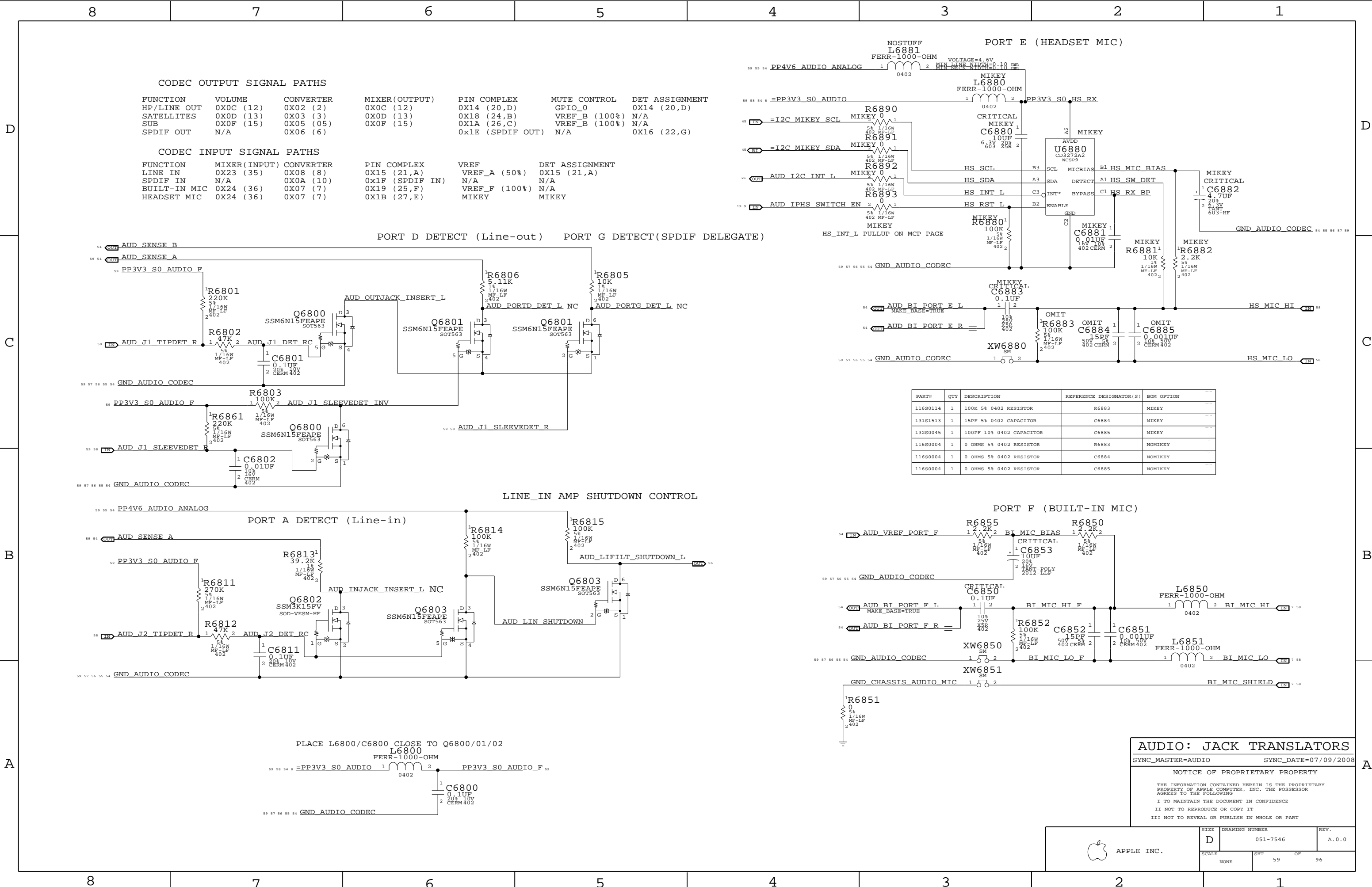
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	58	96



CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SATELLITES	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SUB	0X0F (15)	0X05 (05)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)		0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
BUILT-IN MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT D DETECT (Line-out) PORT G DETECT (SPDIF DELEGATE)

PORT E (HEADSET MIC)

PORT F (BUILT-IN MIC)

PORT A DETECT (Line-in)

LINE_IN AMP SHUTDOWN CONTROL

PLACE L6800/C6800 CLOSE TO Q6800/01/02

AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

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APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7546

A.0.0

SCALE

SHT

OF

96

NONE

59

96


D

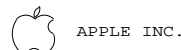


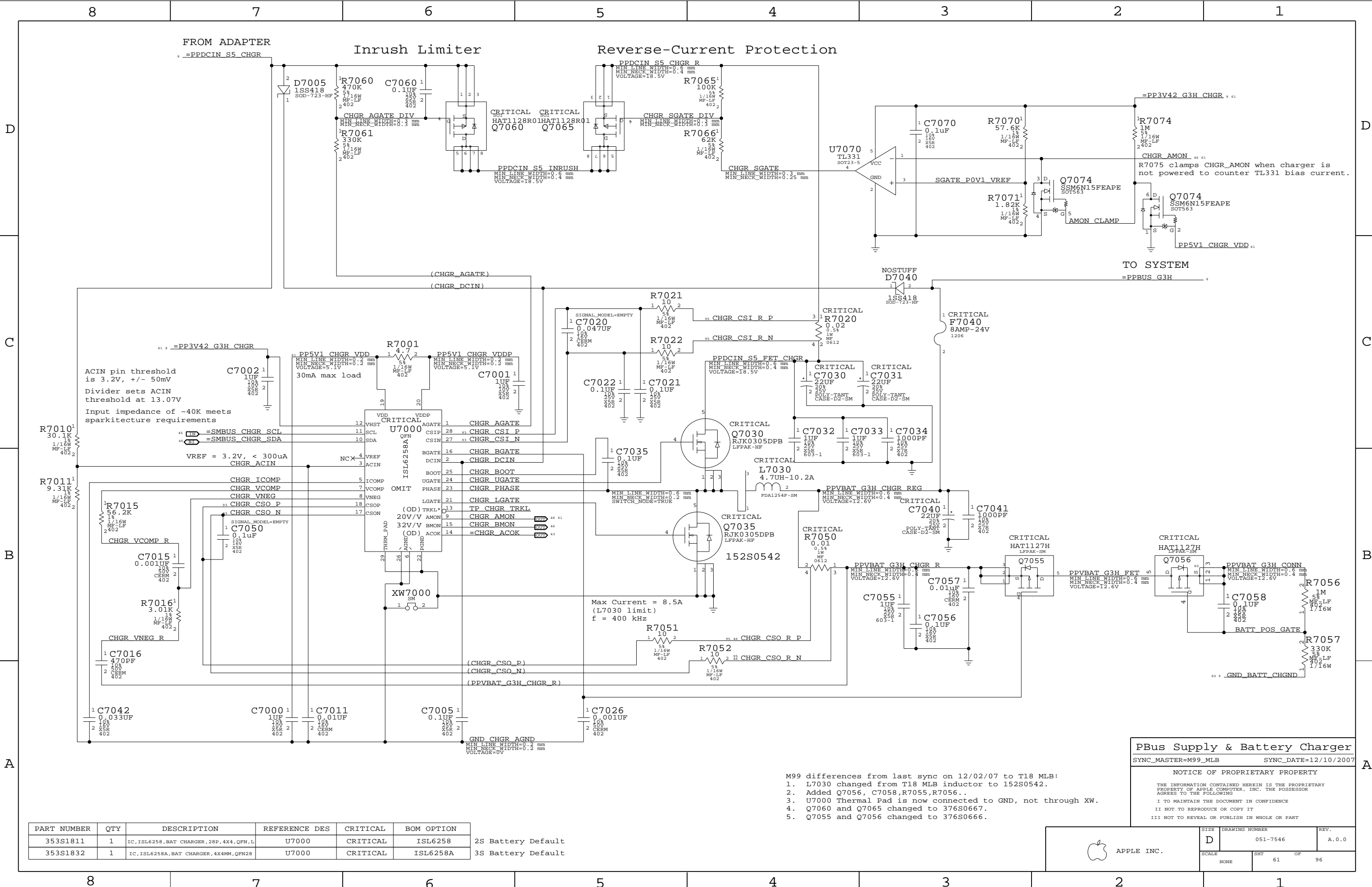
B

A



 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
	SCALE	SHT OF	
	NONE	60 96	





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1811	1	IC, ISL6258, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	ISL6258
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	ISL6258A

2S Battery Default
3S Battery Default

- M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
 2. Added Q7056, C7058, R7055, R7056..
 3. U7000 Thermal Pad is now connected to GND, not through XW.
 4. Q7060 and Q7065 changed to 376S0667.
 5. Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger

SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

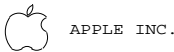
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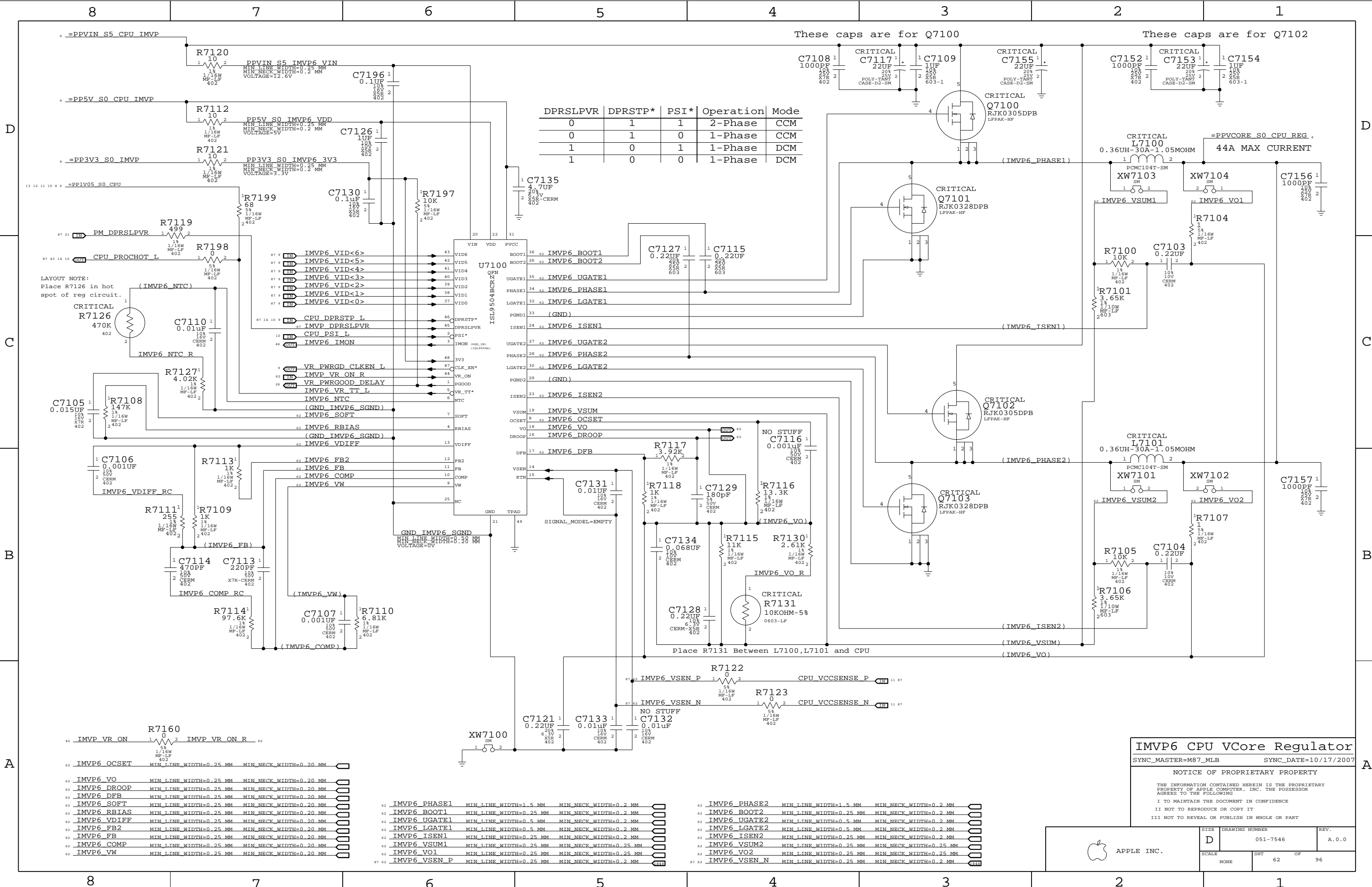
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	61	96



IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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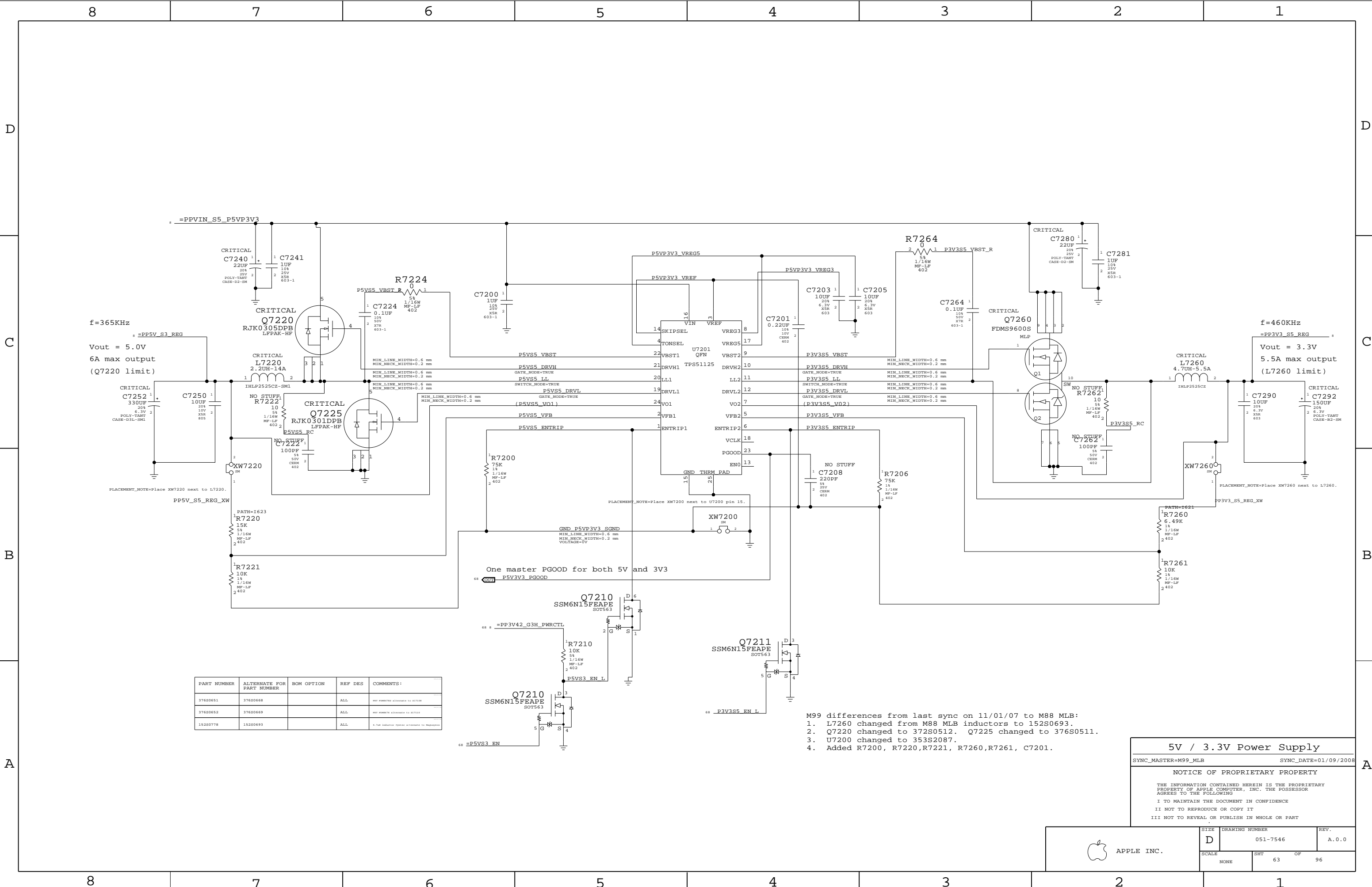
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APPLE INC.

SIZE D DRAWING NUMBER 051-7546 REV. A.0.0

SCALE NONE SHT 62 OF 96

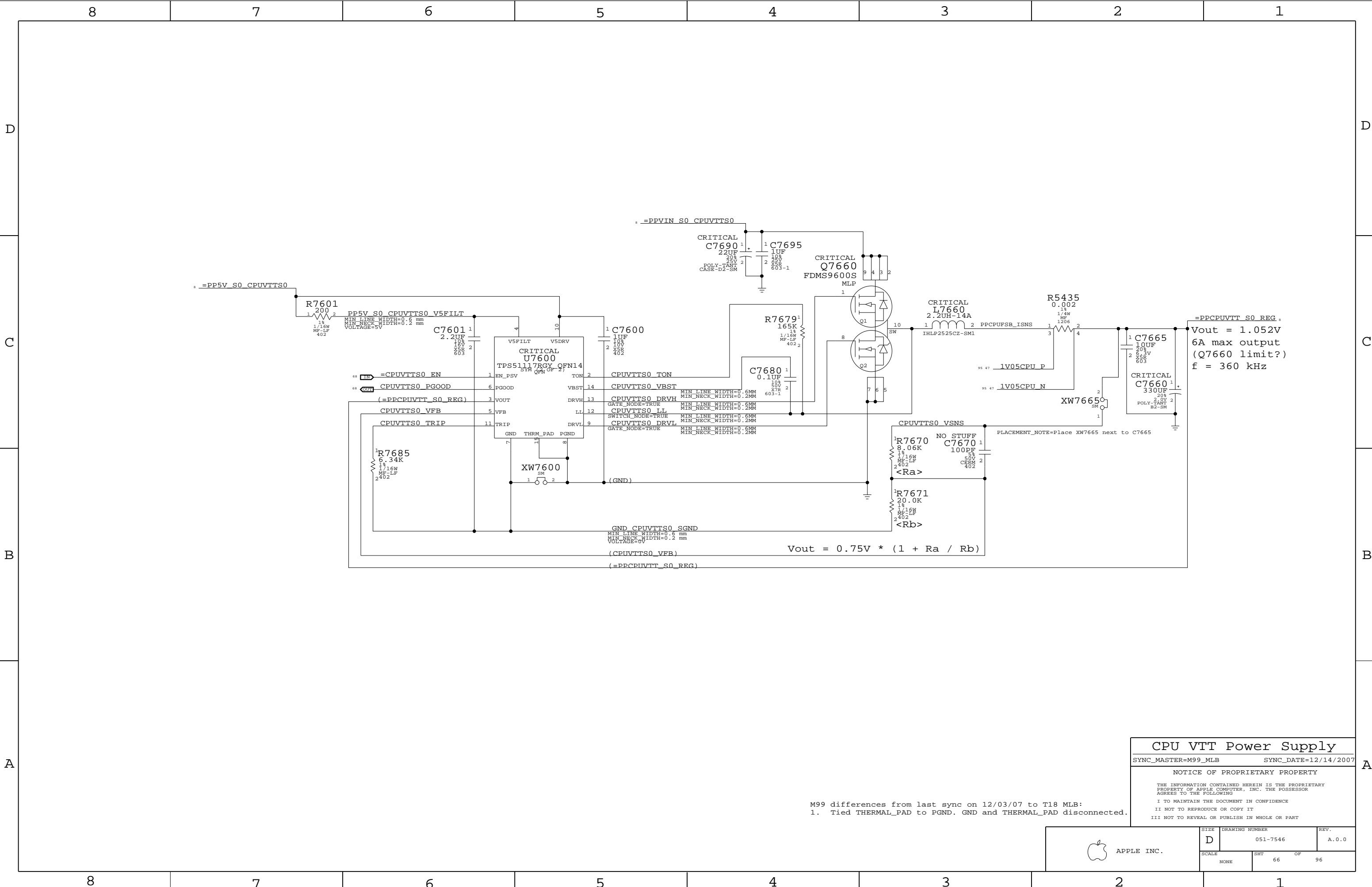


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680651	37680668		ALL	REV FORMERLY ASSIGNED TO 81708
37680652	37680669		ALL	REV FORMERLY ASSIGNED TO 81710
15280778	15280693		ALL	A Thin Inductive Output Inductor to Regulator

M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220, R7221, R7260, R7261, C7201.

5V / 3.3V Power Supply	
SYNC_MASTER=M99_MLB	SYNC_DATE=01/09/2008
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	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		63	96



M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

CPU VTT Power Supply

SYNC_MASTER=M99_MLB

SYNC_DATE=12/14/2007

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

NONE

SHT

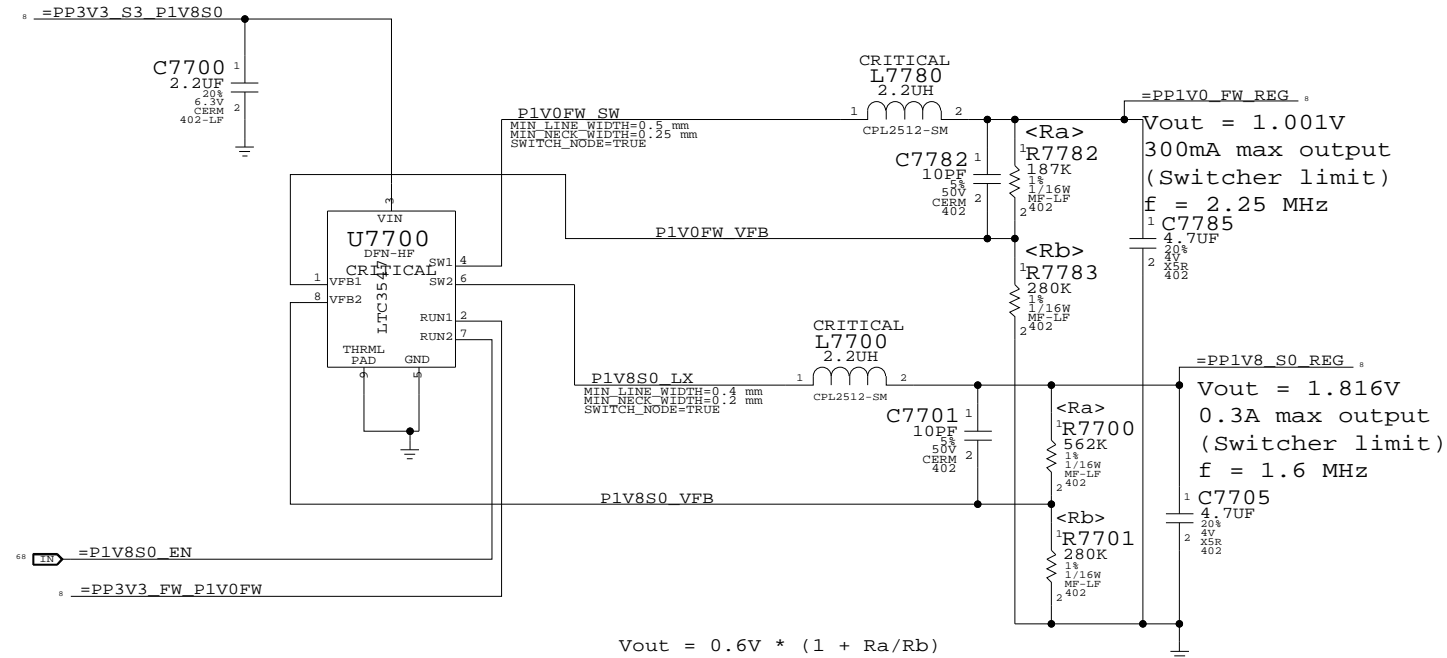
66

OF

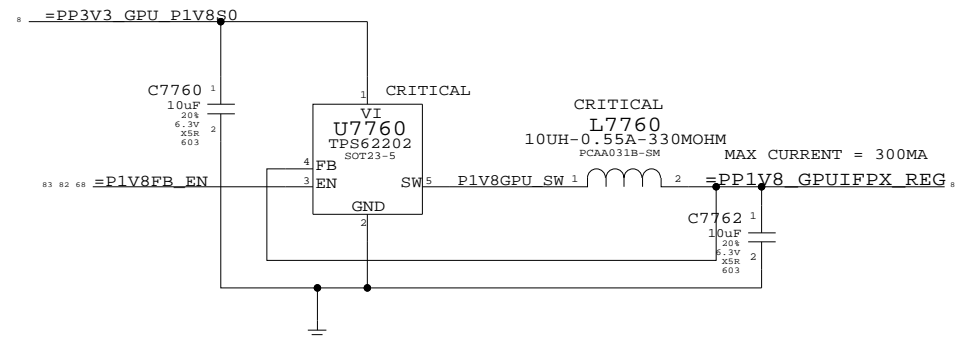
96

1.8V S0 Switcher / 1.0VFW SWITCHER

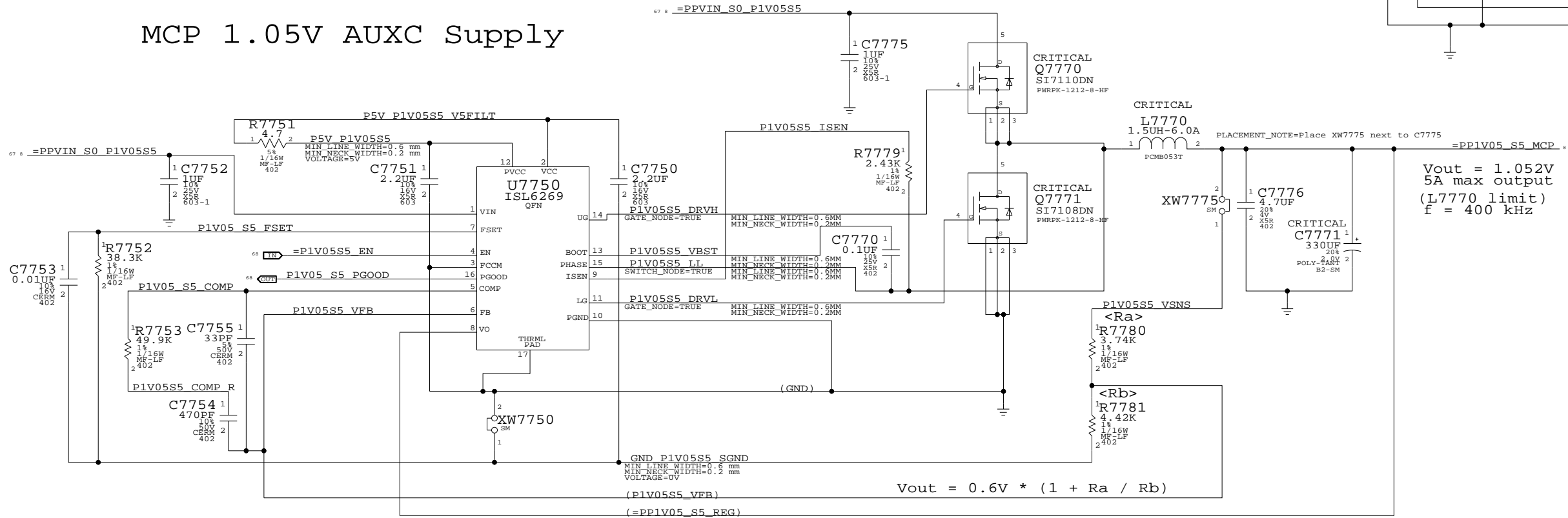
S5 power required for output discharge feature



1.8V S0 Switcher



MCP 1.05V AUXC Supply



Misc Power Supplies

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

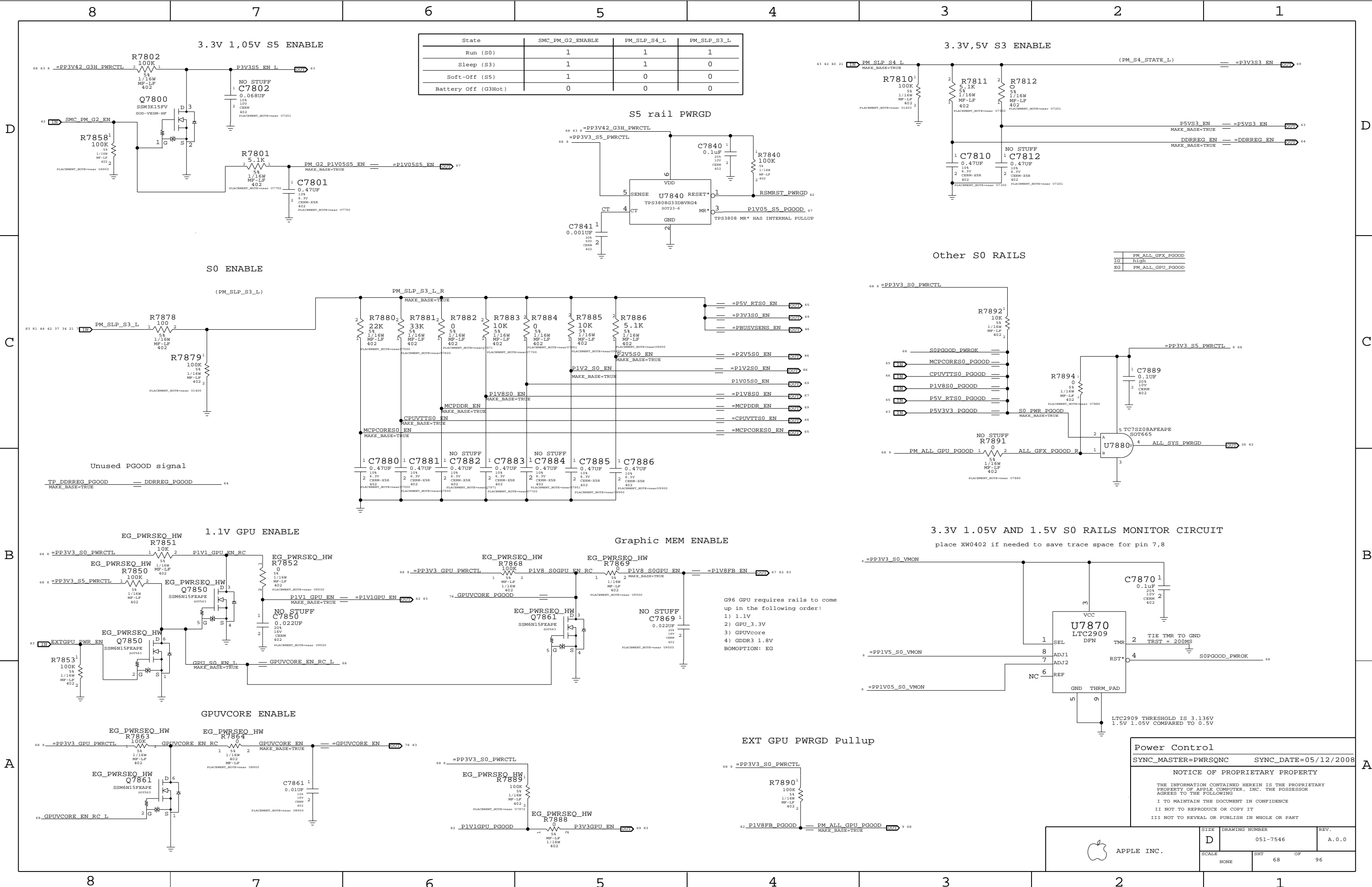
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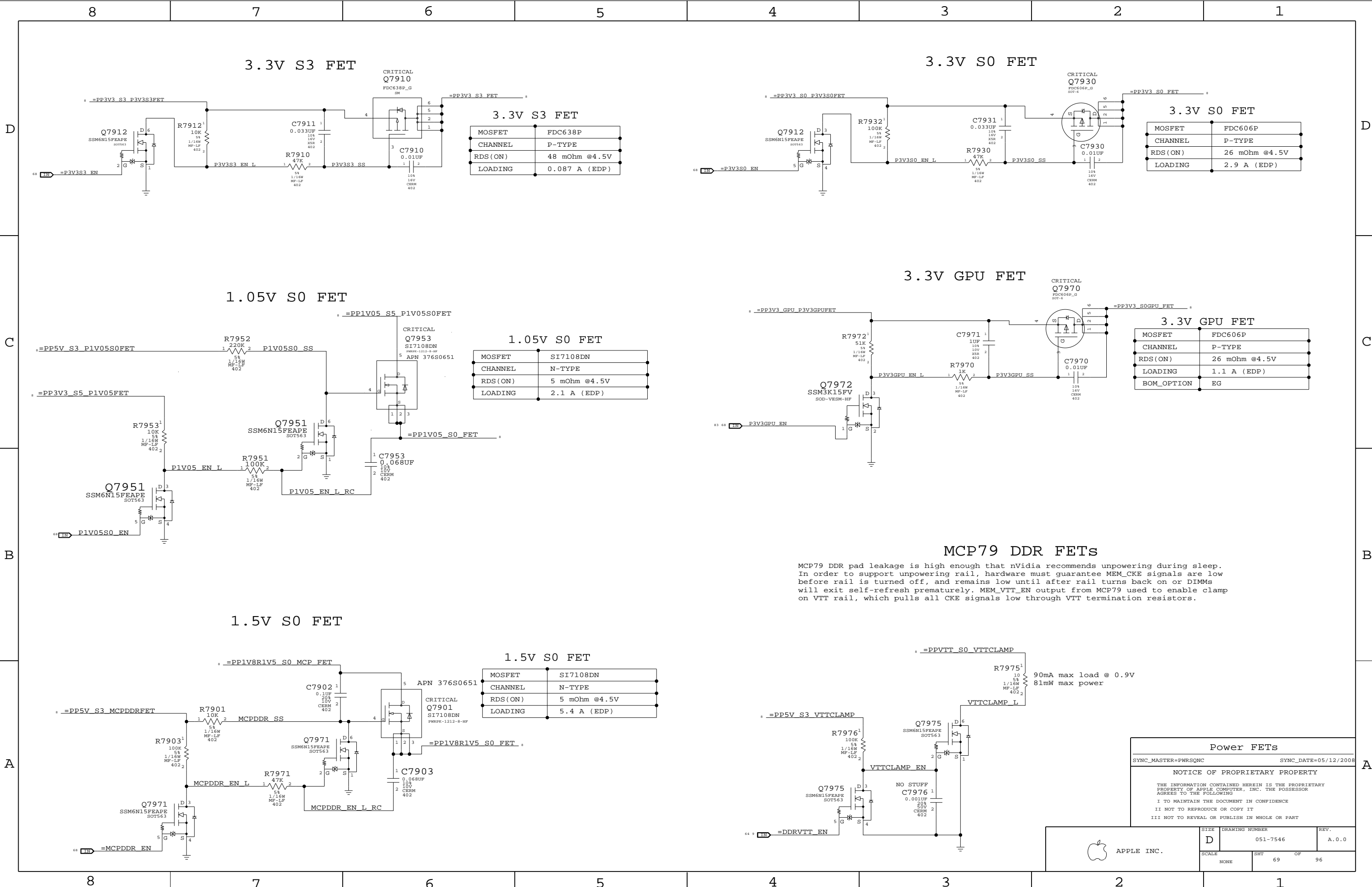
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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	67	96





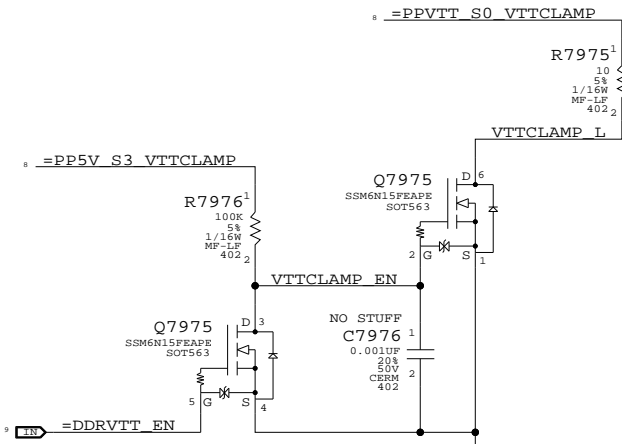
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	2.1 A (EDP)

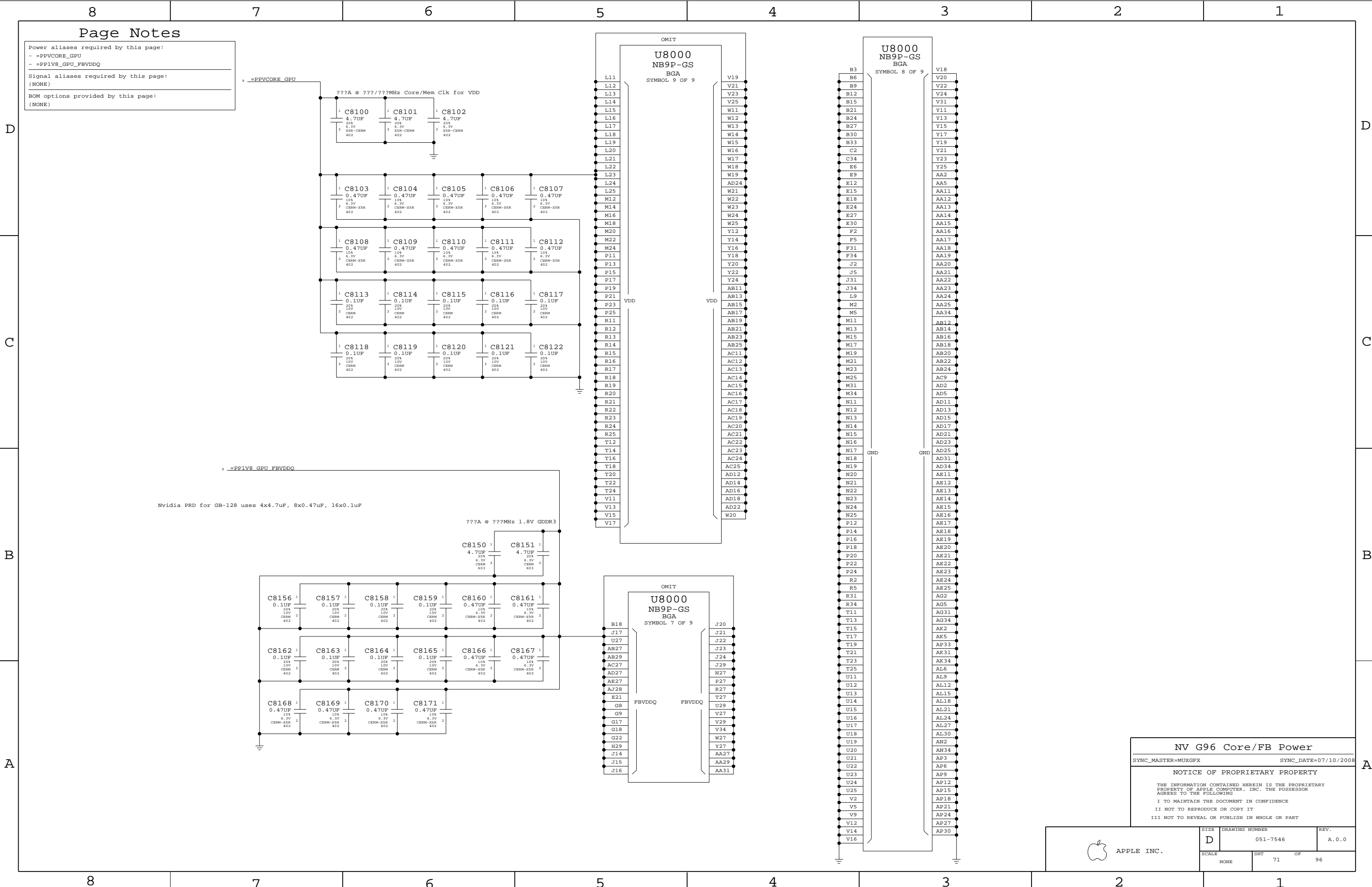
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

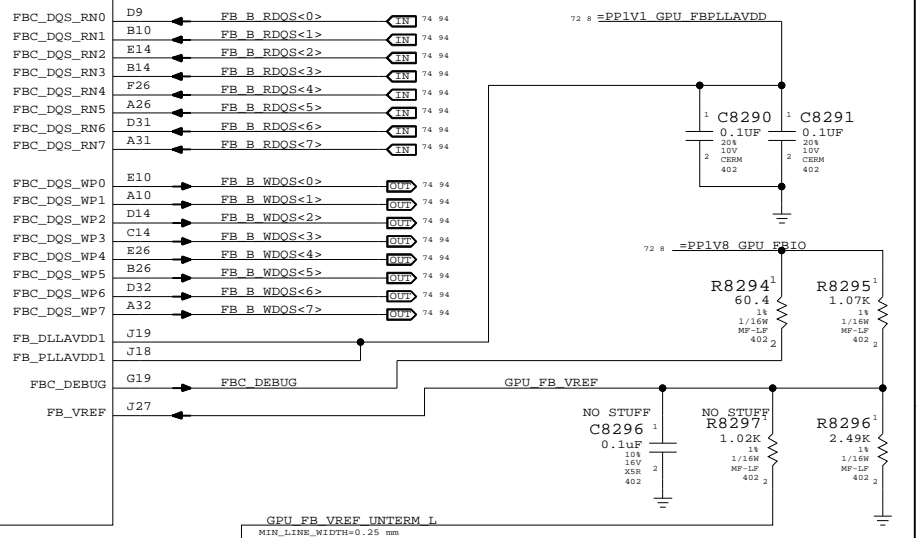
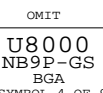
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)



Power FETs		
SYNC_MASTER=PWRSQNC		SYNC_DATE=05/12/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	69 OF 96
NONE			





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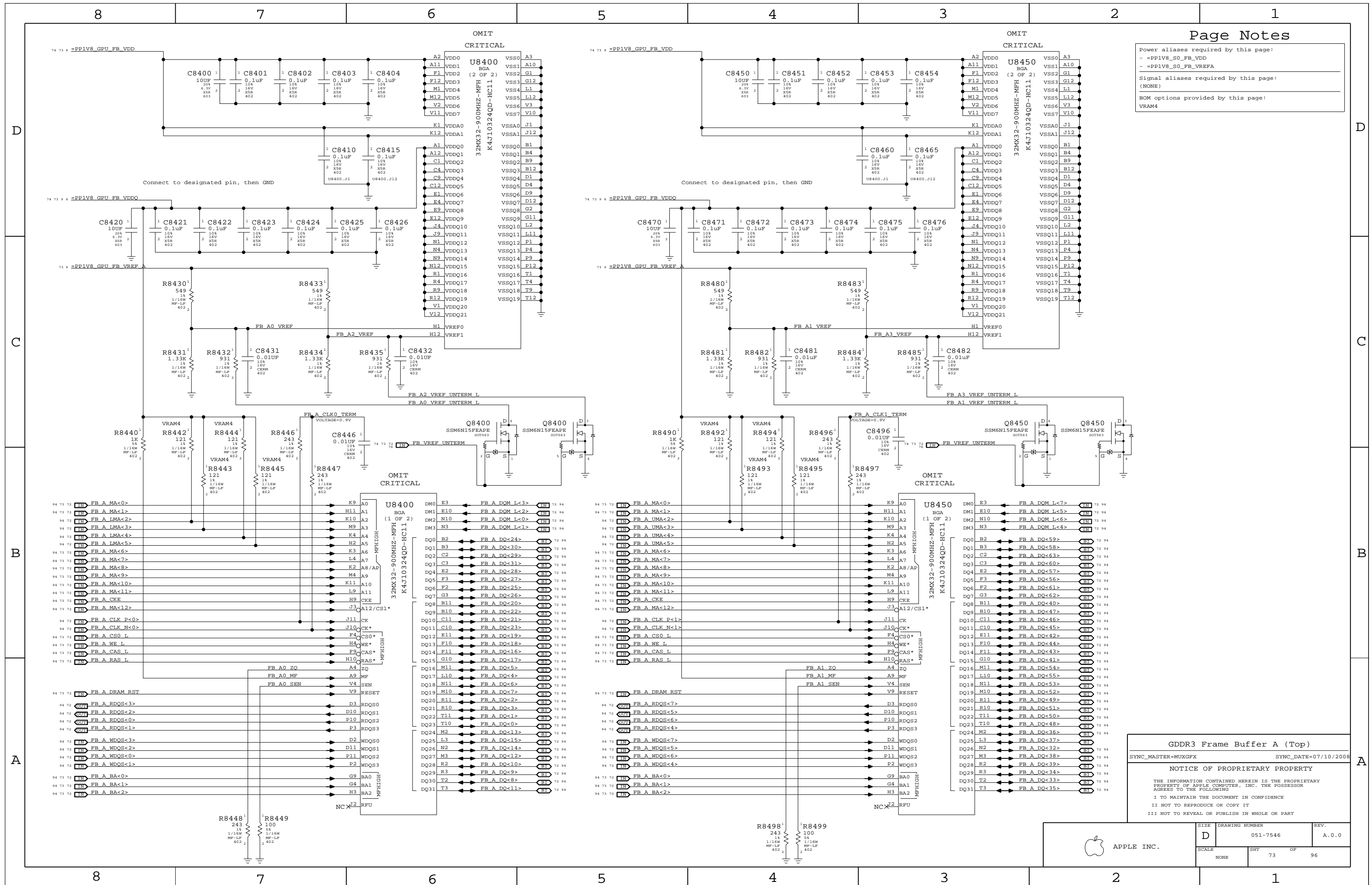
NV G96 Frame Buffer I/F
-----
SYNC_MASTER=MUXGFX                               SYNC_DATE=07/10/2008

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1

Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD

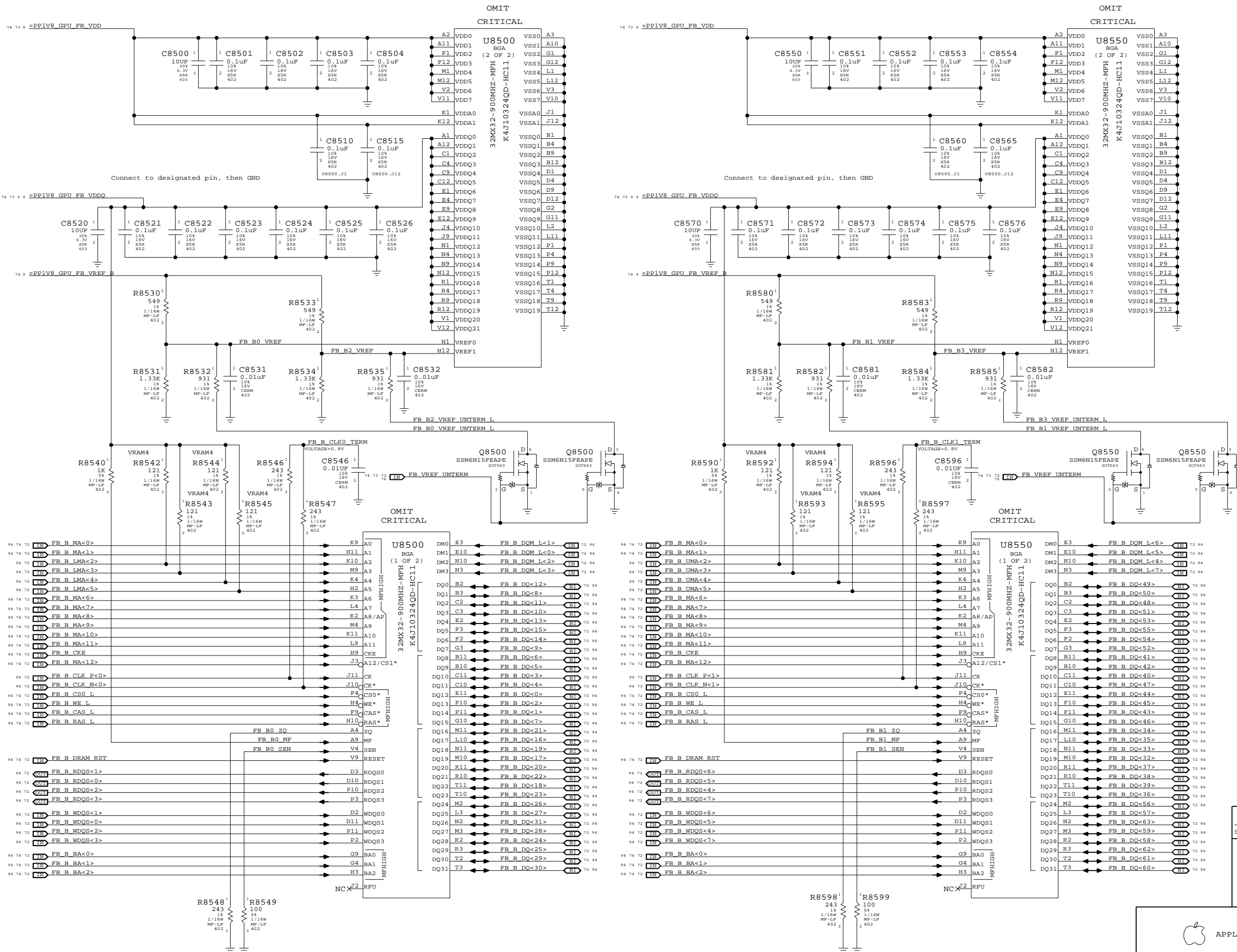
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4



GDDR3 Frame Buffer B (Top)

SYNC_MASTER=MUXGFX

SYNC_DATE=07/10/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

NONE

SIT

74

OF

96

Power aliases required by this page:

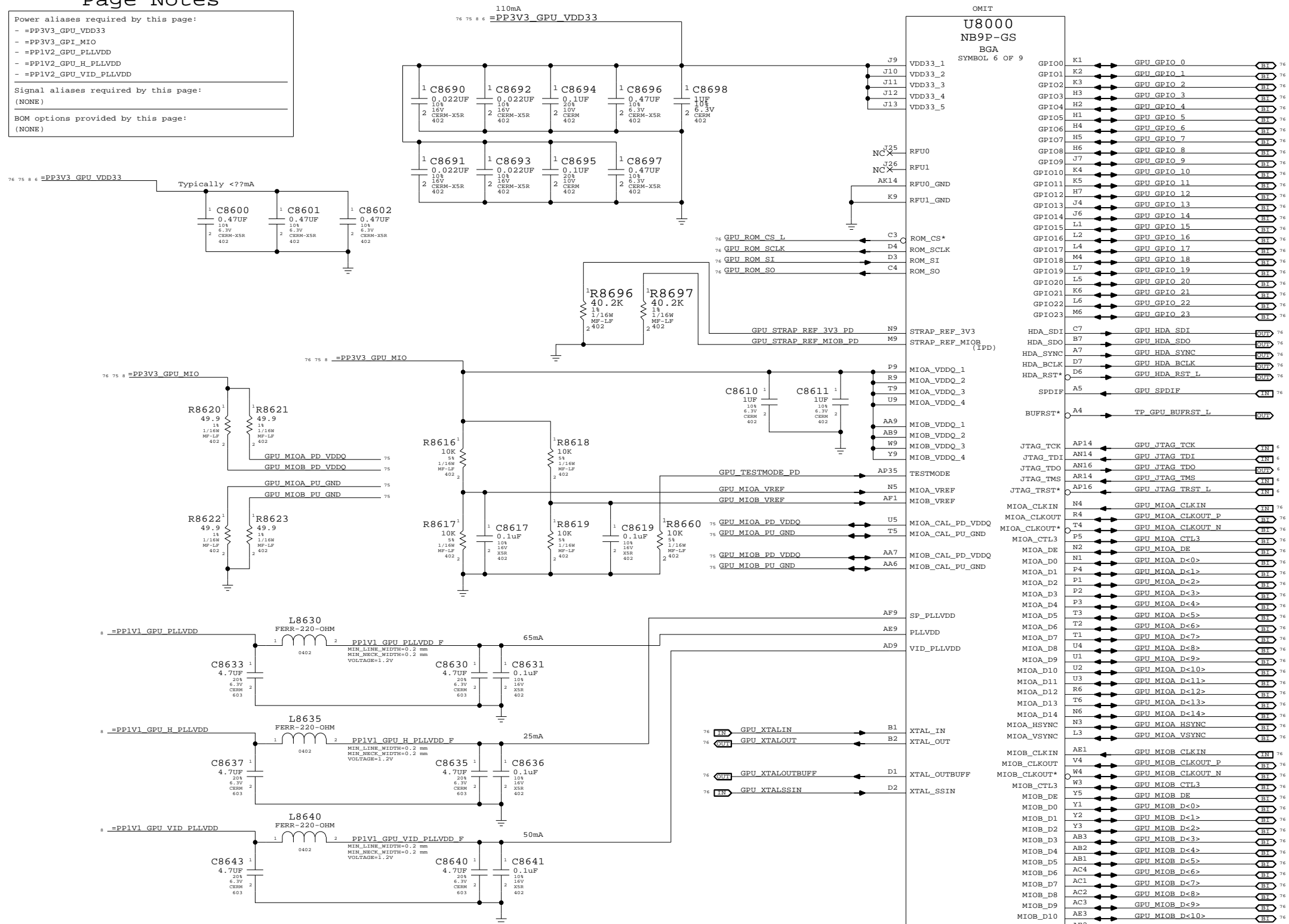
- PP3V3_GPU_VDD33
- PP3V3_GPU_MIO
- PP1V2_GPU_PLLVDD
- PP1V2_GPU_H_PLLVDD
- PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



LP 9	GPI00	K1	GPU GPIO 0	B3	76
	GPI01	K2	GPU GPIO 1	B3	76
	GPI02	K3	GPU GPIO 2	B3	76
	GPI03	H3	GPU GPIO 3	B3	76
	GPI04	H2	GPU GPIO 4	B3	76
	GPI05	H1	GPU GPIO 5	B3	76
	GPI06	H4	GPU GPIO 6	B3	76
	GPI07	H5	GPU GPIO 7	B3	76
	GPI08	H6	GPU GPIO 8	B3	76
	GPI09	J4	GPU GPIO 9	B3	76
	GPI010	K4	GPU GPIO 10	B3	76
	GPI011	K5	GPU GPIO 11	B3	76
	GPI012	H7	GPU GPIO 12	B3	76
	GPI013	J4	GPU GPIO 13	B3	76
	GPI014	J1	GPU GPIO 14	B3	76
	GPI015	L1	GPU GPIO 15	B3	76
	GPI016	L2	GPU GPIO 16	B3	76
	GPI017	L4	GPU GPIO 17	B3	76
	GPI018	M4	GPU GPIO 18	B3	76
	GPI019	L7	GPU GPIO 19	B3	76
	GPI020	L5	GPU GPIO 20	B3	76
	GPI021	K6	GPU GPIO 21	B3	76
	GPI022	L6	GPU GPIO 22	B3	76
	GPI023	M6	GPU GPIO 23	B3	76
	HDA_SDI	C7	GPU HDA SDI	DA16	76
	HDA_SDO	B7	GPU HDA SDO	DA16	76
	HDA_SYNC	A7	GPU HDA SYNC	DA16	76
	HDA_BCLK	D7	GPU HDA BCLK	DA16	76
	HDA_RST*	D6	GPU HDA RST L	DA16	76
	SPDIF	A5	GPU SPDIF	DA16	76
	BUFRST*	A4	TP GPU BUFRST L	DA16	76
	JTAG_TCK	AP14	GPU JTAG TCK	DA16	76
	JTAG_TDI	AN14	GPU JTAG TDI	DA16	76
	JTAG_TDO	AN16	GPU JTAG TDO	DA16	76
	JTAG_TMS	AR14	GPU JTAG TMS	DA16	76
	JTAG_TRST*	AP16	GPU JTAG TRST L	DA16	76
	MIOA_CLKIN	N4	GPU MIOA CLKIN	B3	76
	MIOA_CLKOUT	R4	GPU MIOA_CLKOUT P	B3	76
	MIOA_CLKOUT*	T4	GPU MIOA_CLKOUT N	B3	76
	MIOA_CTL3	P5	GPU MIOA_CTL3	B3	76
	MIOA_DE	N2	GPU MIOA DE	B3	76
	MIOA_D0	N1	GPU MIOA D<0>	B3	76
	MIOA_D1	P1	GPU MIOA D<1>	B3	76
	MIOA_D2	P4	GPU MIOA D<2>	B3	76
	MIOA_D3	P2	GPU MIOA D<3>	B3	76
	MIOA_D4	P3	GPU MIOA D<4>	B3	76
	MIOA_D5	T3	GPU MIOA D<5>	B3	76
	MIOA_D6	T2	GPU MIOA D<6>	B3	76
	MIOA_D7	T1	GPU MIOA D<7>	B3	76
	MIOA_D8	U4	GPU MIOA D<8>	B3	76
	MIOA_D9	U1	GPU MIOA D<9>	B3	76
	MIOA_D10	U2	GPU MIOA D<10>	B3	76
	MIOA_D11	U3	GPU MIOA D<11>	B3	76
	MIOA_D12	R6	GPU MIOA D<12>	B3	76
	MIOA_D13	T6	GPU MIOA D<13>	B3	76
	MIOA_D14	N6	GPU MIOA D<14>	B3	76
	MIOA_HSVNC	N3	GPU MIOA HSVNC	B3	76
	MIOA_VSVNC	L3	GPU MIOA VSVNC	B3	76
	MI0B_CLKIN	AE1	GPU MI0B CLKIN	B3	76
	MI0B_CLKOUT	V4	GPU MI0B_CLKOUT P	B3	76
	MI0B_CLKOUT*	W4	GPU MI0B_CLKOUT N	B3	76
	MI0B_CTL3	W3	GPU MI0B_CTL3	B3	76
	MI0B_DE	Y5	GPU MI0B DE	B3	76
	MI0B_D0	Y1	GPU MI0B D<0>	B3	76
	MI0B_D1	Y2	GPU MI0B D<1>	B3	76
	MI0B_D2	Y3	GPU MI0B D<2>	B3	76
	MI0B_D3	AB3	GPU MI0B D<3>	B3	76
	MI0B_D4	AB2	GPU MI0B D<4>	B3	76
	MI0B_D5	AB1	GPU MI0B D<5>	B3	76
	MI0B_D6	AC4	GPU MI0B D<6>	B3	76
	MI0B_D7	AC1	GPU MI0B D<7>	B3	76
	MI0B_D8	AC2	GPU MI0B D<8>	B3	76
	MI0B_D9	AC3	GPU MI0B D<9>	B3	76
	MI0B_D10	AE3	GPU MI0B D<10>	B3	76
	MI0B_D11	AE2	GPU MI0B D<11>	B3	76
	MI0B_D12	U6	GPU MI0B D<12>	B3	76
	MI0B_D13	W6	GPU MI0B D<13>	B3	76
	MI0B_D14	Y6	GPU MI0B D<14>	B3	76
	MI0B_D15	W5	GPU STRAP<0>	B3	76
	MI0B_D16	W7	GPU STRAP<1>	B3	76
	MI0B_D17	V7	GPU STRAP<2>	B3	76
	MI0B_HSVNC	W1	GPU MI0B HSVNC	B3	76
	MI0B_VSVNC	W2	GPU MI0B VSVNC	B3	76
	THERMDP	B5	GPU THERMD P	DA16	76
	THERMDN	B4	GPU THERMD N	DA16	76
	PGOOD_OUT*	C5	TP GPU PGOOD OUT L	DA16	76

NV G96 GPIO/MIO/Misc	
SYNC_MASTER=MUXGFX	SYNC_DATE=07/10/2008
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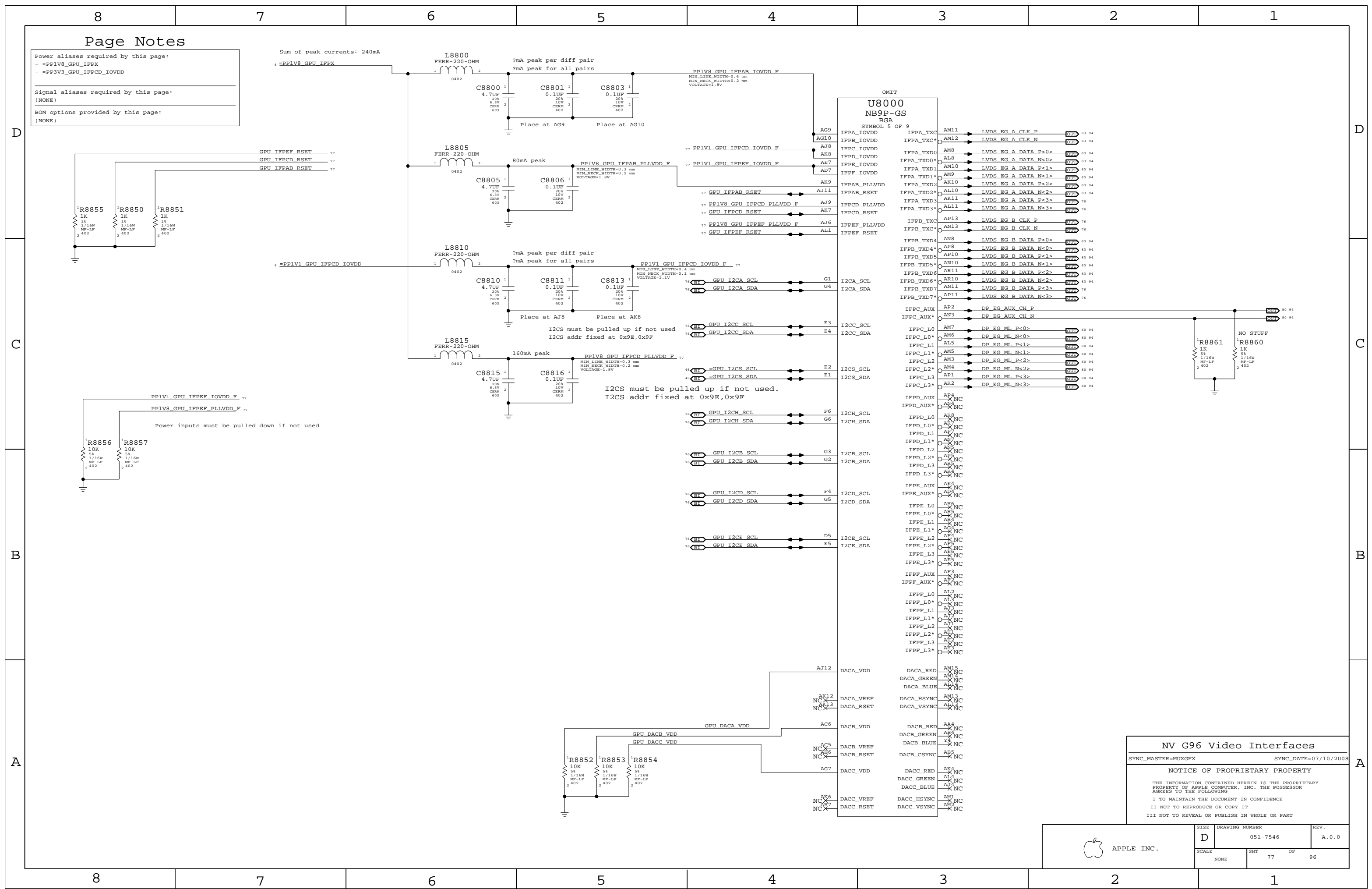
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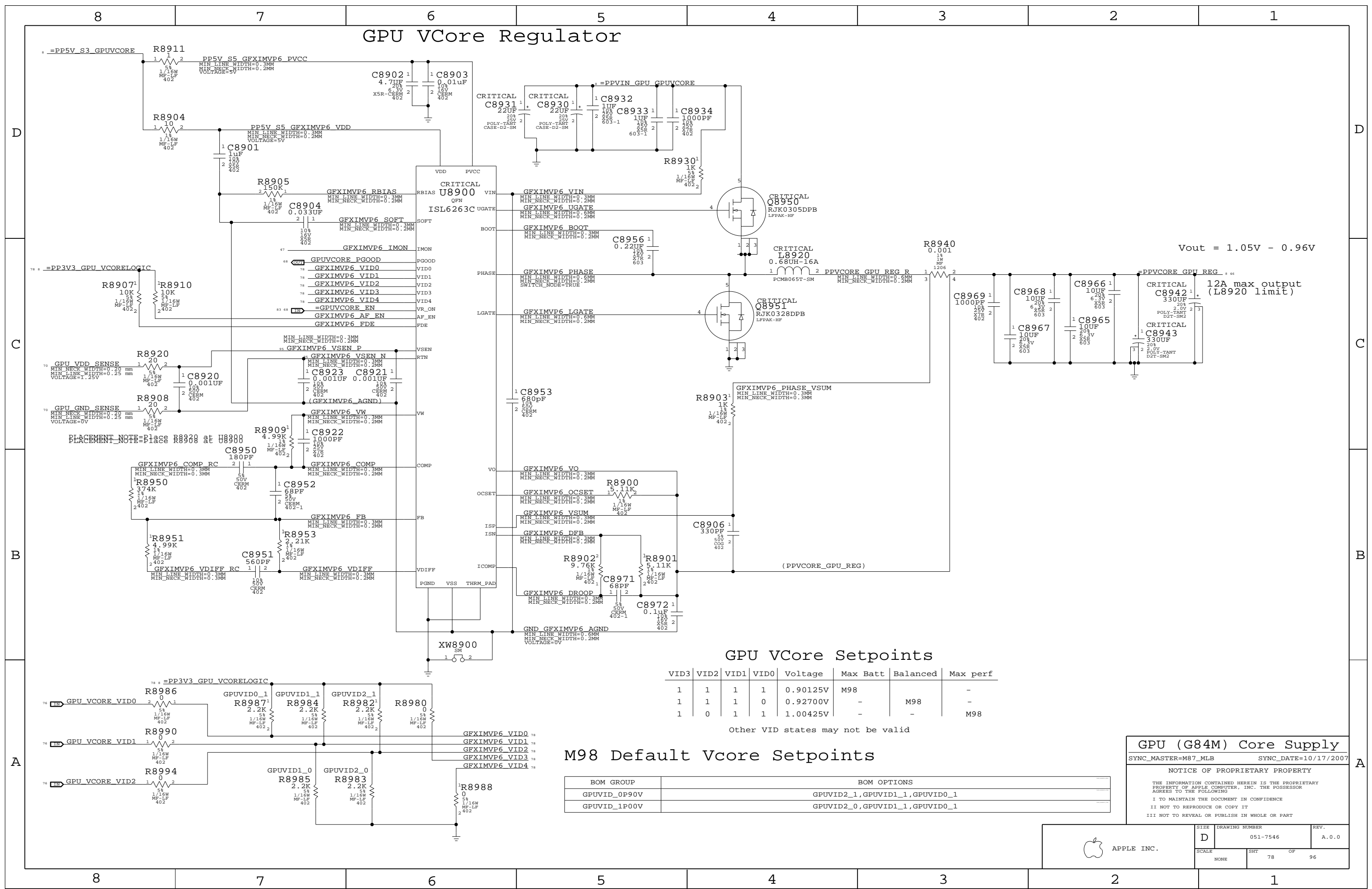


NV G96 Video Interfaces	
SYNCH_MASTER=MUXGFX	SYNCH_DATE=07/10/2008
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SCALE NONE	SHT 77	OF 96



VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	M98		-
1	1	1	0	0.92700V	-	M98	-
1	0	1	1	1.00425V	-	-	M98

M98 Default Vcore Setpoints

GPU (G84M) Core Supply

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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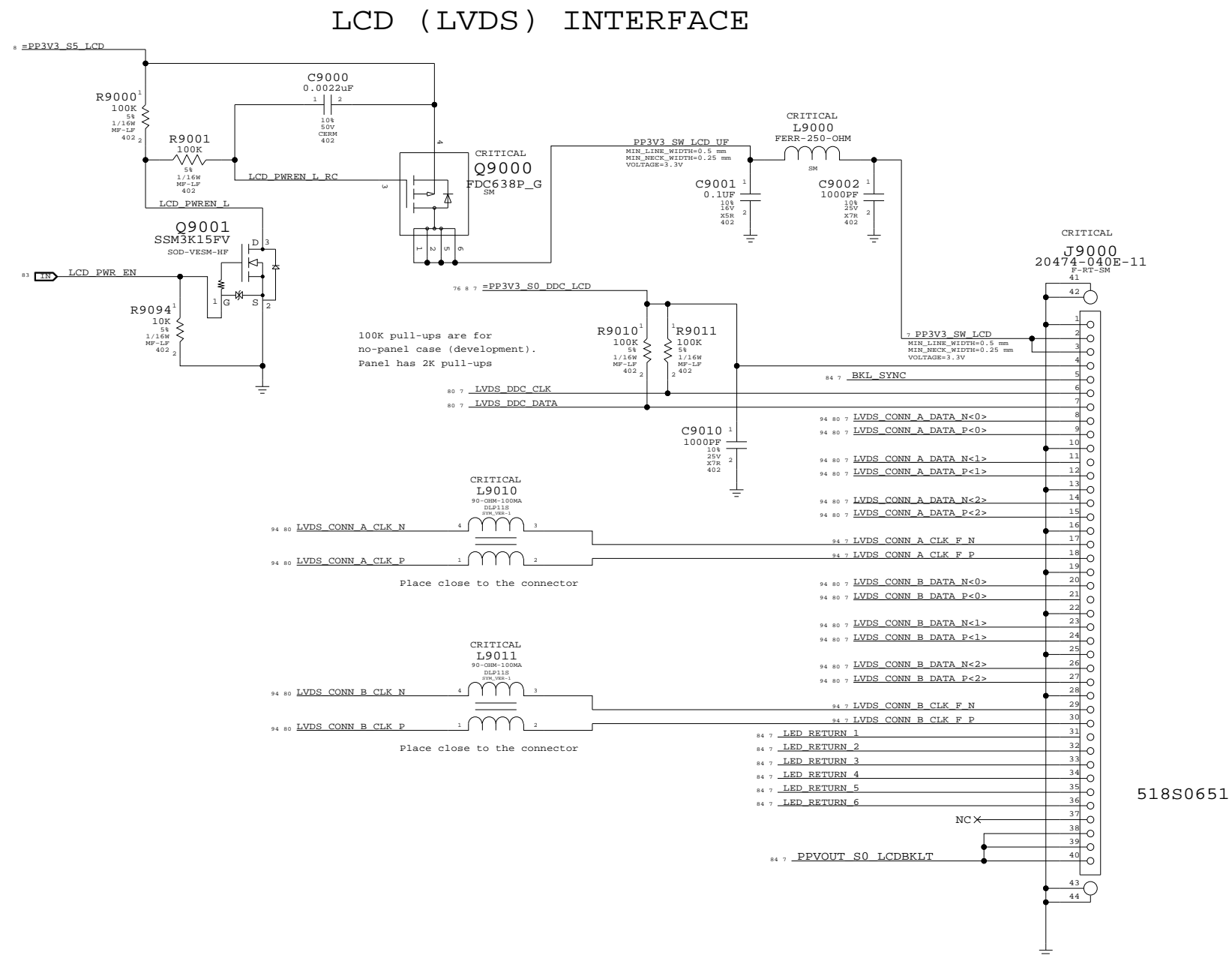
	SIZE	DRAWING NUMBER	RI
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D	051-7546
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SCALE	SHT	OF	


NONE	78	96
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518S0651

LVDS Display Connector	
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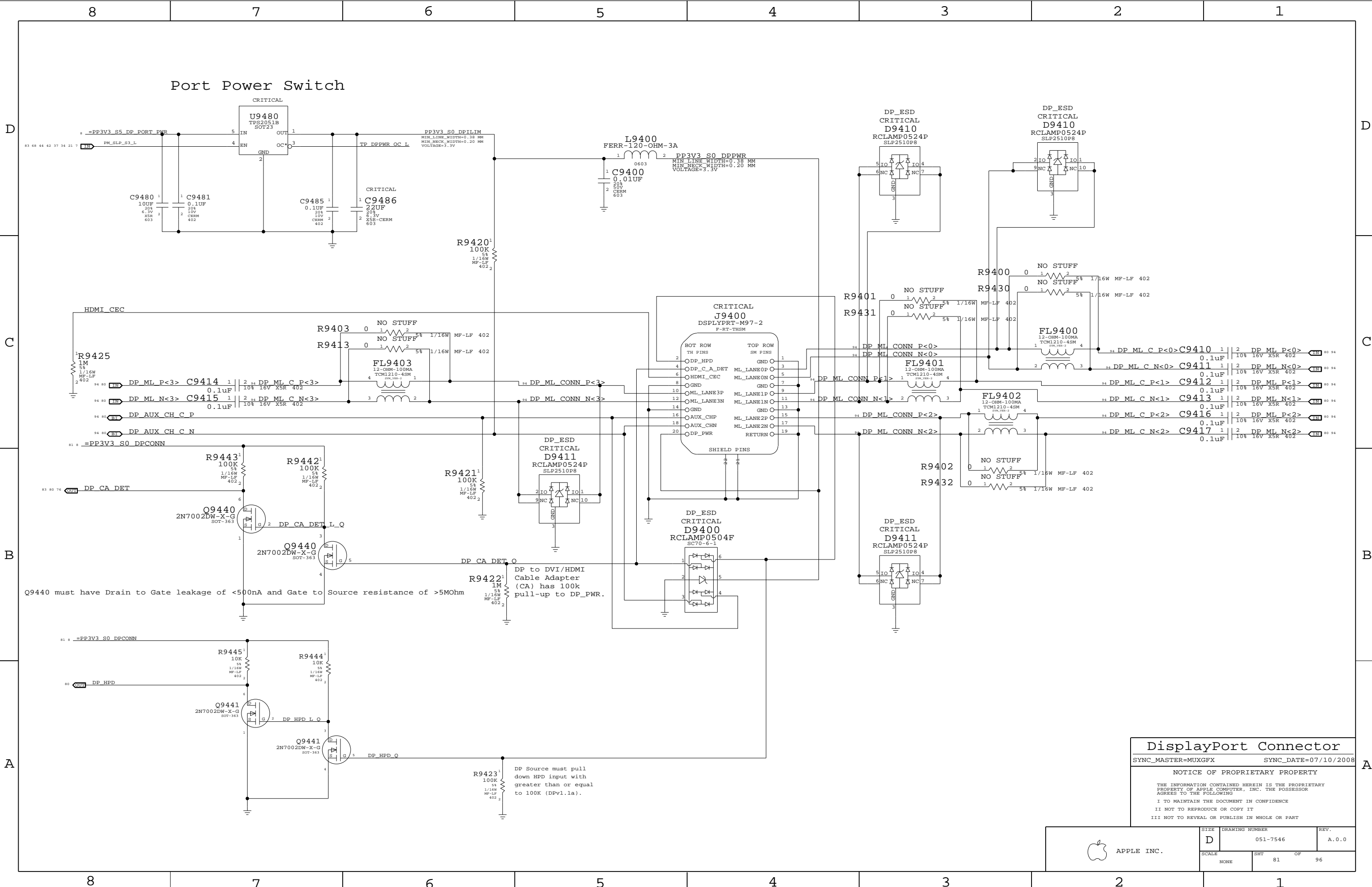
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SCALE	SHT	OF
NONE	80	96



DisplayPort Connector

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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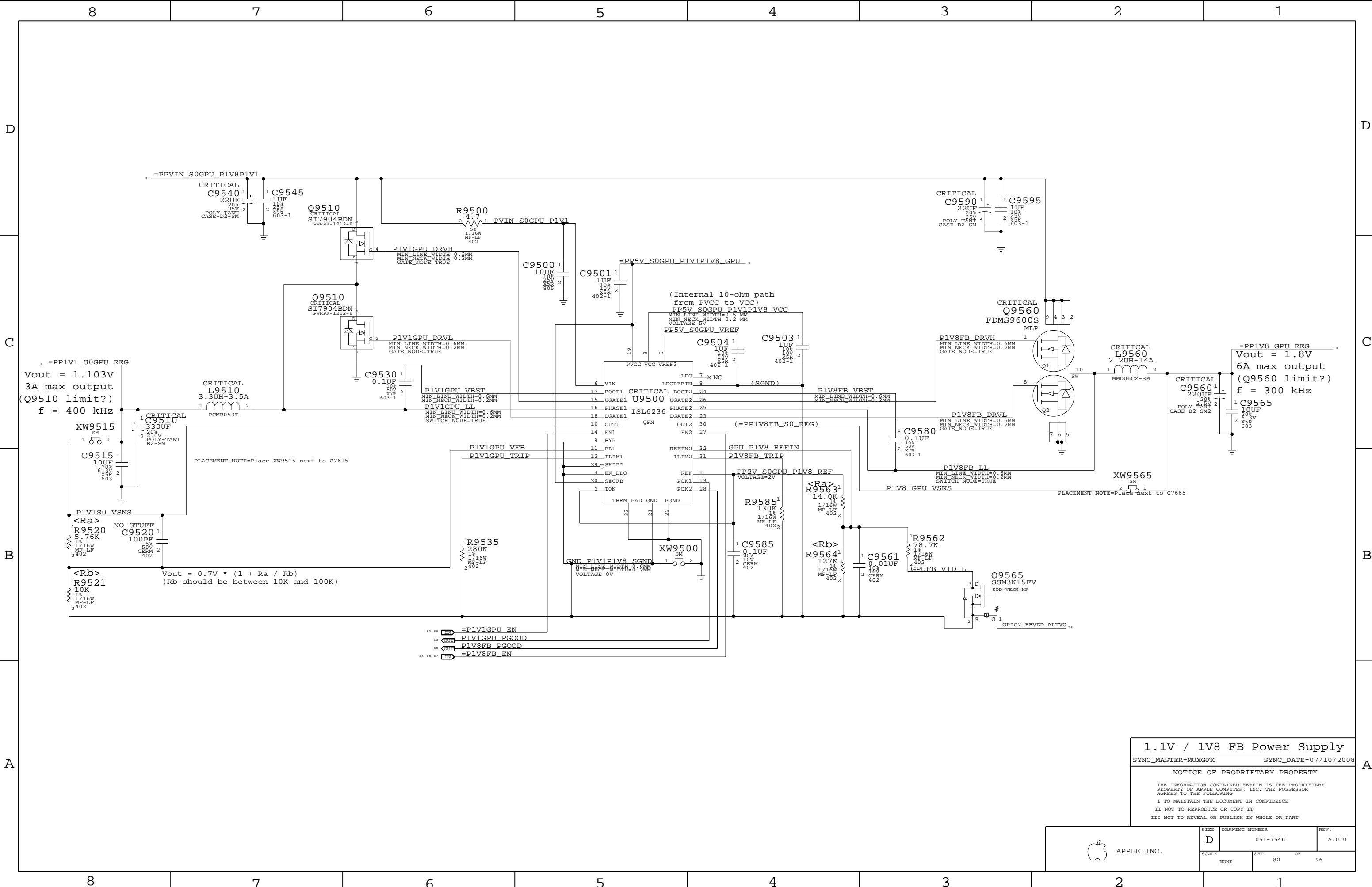
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SCALE	SHT	OF
NONE	81	96



1.1V / 1V8 FB Power Supply

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

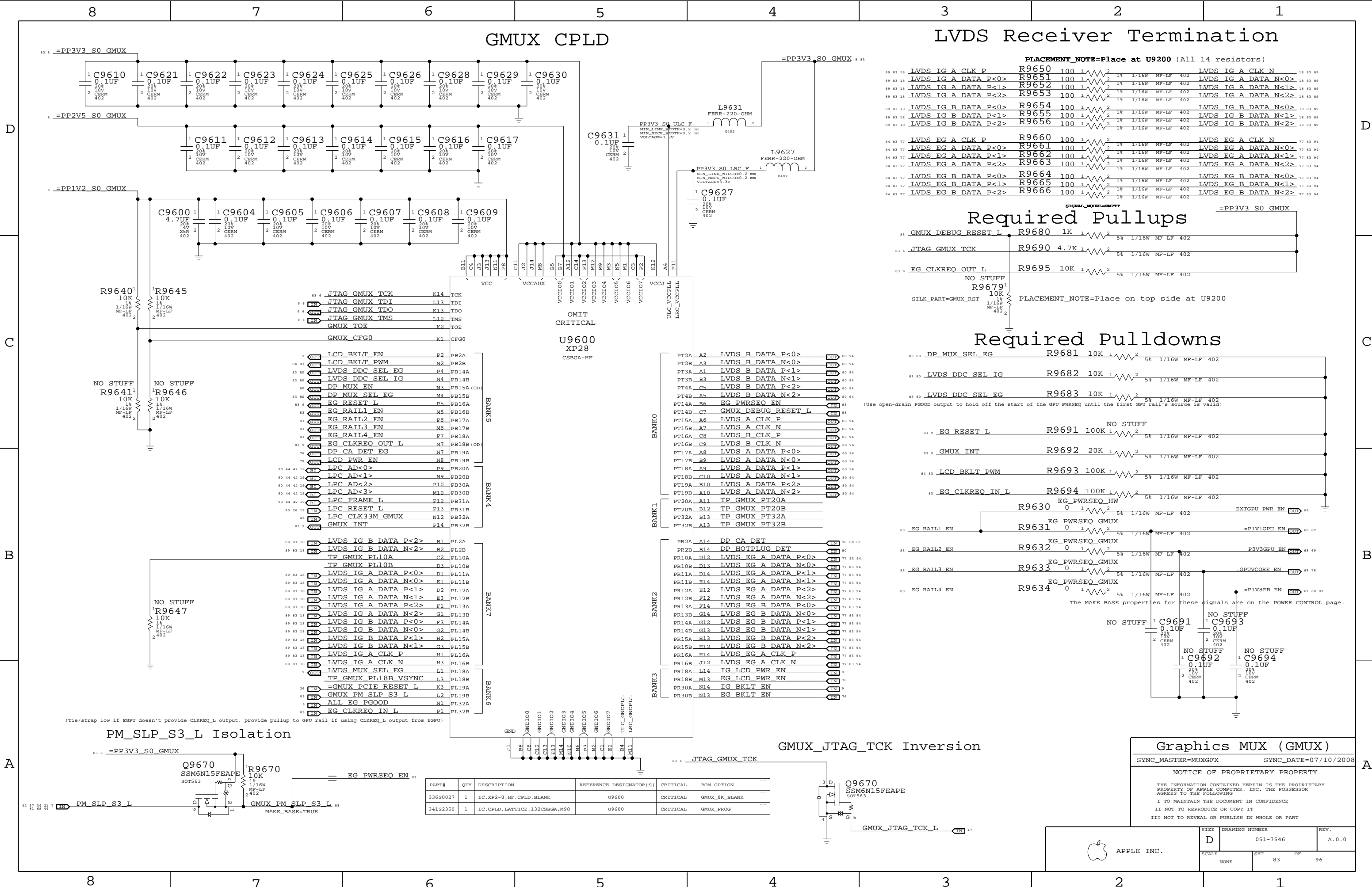
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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	82	96



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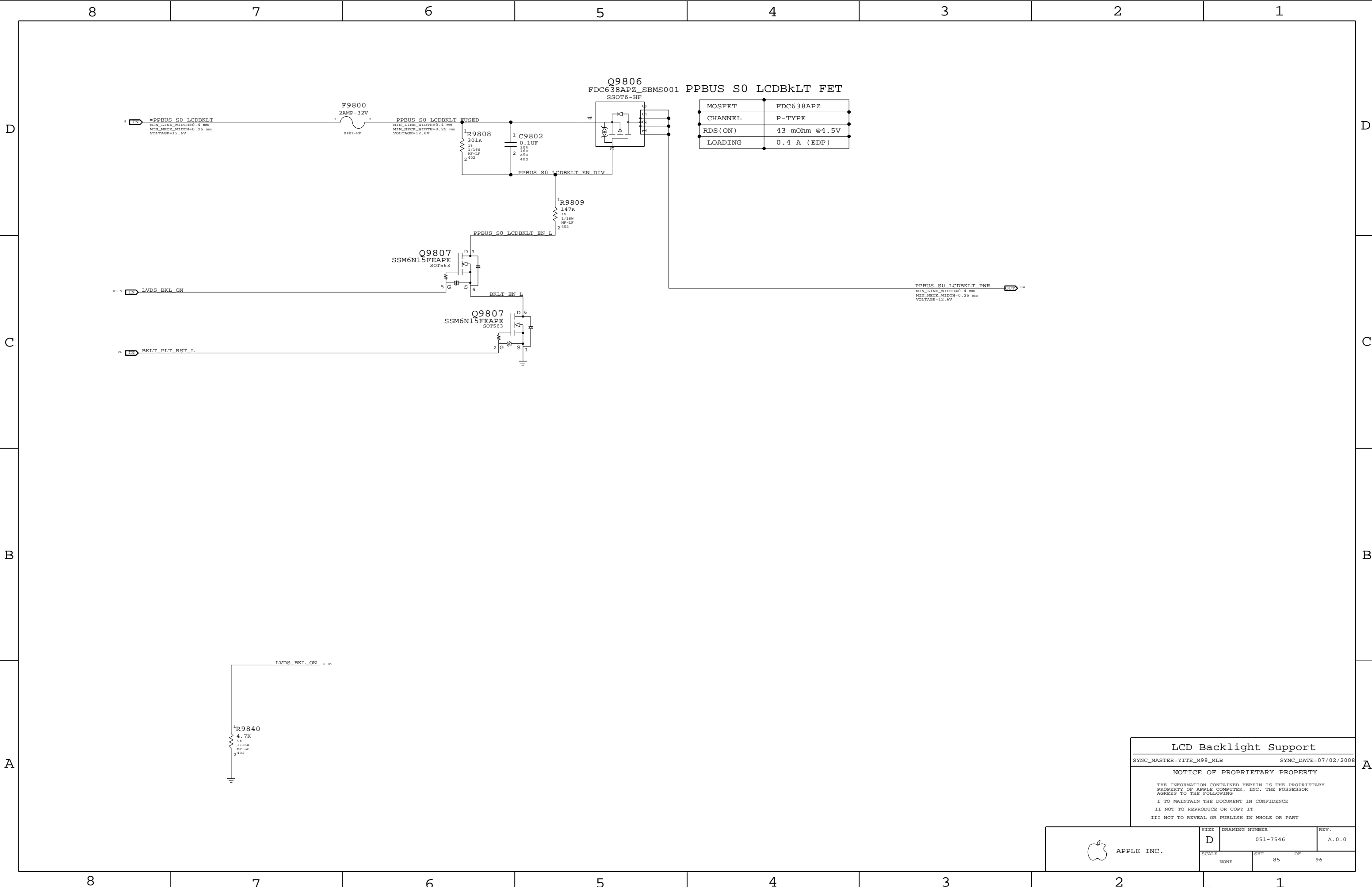
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LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB

SYNC_DATE=07/02/2008


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SCALE		SHT	OF	
NONE		85	96	

2.5V/1.2V S3 Switcher

$$V_{out} = 0.6V * (1 + R_a/R_b)$$

<h1>Misc Power Supplies</h1>	
SYNC_MASTER=MUXGFX	SYNC_DATE=02/01/2008
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	SCALE NONE	SHT 86 OF 96	

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS_L<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS_L<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16

Memory Constraints

SYNC_MASTER=MUXGFX

SYNC_DATE=02/18/2008

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1

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	MCP_DEBUG	PCT_55S	PCT	MCP_DEBUG<7..0>	13 19
	PCI_AD	PCT_55S	PCI	PCI_AD<23..8>	
	PCI_AD24	PCT_55S	PCI	PCI_AD<24>	
	PCI_AD	PCT_55S	PCI	PCI_AD<31..25>	
	PCI_AD	PCT_55S	PCI	PCI_PAR	
	PCI_C_BE_L	PCT_55S	PCI	PCI_C_BE_L<3..0>	
	PCI_CNTRL	PCT_55S	PCI	PCI_TRDY_L	
	PCI_CNTRL	PCT_55S	PCI	PCI_DEVSEL_L	
	PCI_CNTRL	PCT_55S	PCI	PCI_PERR_L	
	PCI_CNTRL	PCT_55S	PCI	PCI_SERR_L	
	PCI_CNTRL	PCT_55S	PCI	PCI_STOP_L	
	PCI_CNTRL	PCT_55S	PCI	PCI_TRDY_L	
	PCI_CNTRL	PCT_55S	PCI	PCI_FRAME_L	
	PCI_REQ0_L	PCT_55S	PCI	PCI_REQ0_L	19
	PCI_GNT0_L	PCT_55S	PCI	PCI_GNT0_L	
	PCI_REQ1_L	PCT_55S	PCI	PCI_REQ1_L	19
	PCI_GNT1_L	PCT_55S	PCI	PCI_GNT1_L	
	PCI_INTW_L	PCT_55S	PCI	PCI_INTW_L	
	PCI_INTX_L	PCT_55S	PCI	PCI_INTX_L	
	PCI_INTY_L	PCT_55S	PCI	PCI_INTY_L	
	PCI_INTZ_L	PCT_55S	PCI	PCI_INTZ_L	
	MCP_PCT_CLK2	CLK_PCT_55S	CLK_PCT	PCI_CLK33M MCP_R	19
		CLK_PCT_55S	CLK_PCT	PCI_CLK33M MCP	19
	LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 42 44 83
	LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 42 44 83
	LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26 83
	MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R	19 26
		CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC	26 42
		CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS	26 44
	USB_EXT_A	USB_90D	USB	USB_EXT_A_P	20 40
		USB_90D	USB	USB_EXT_A_N	20 40
		USB_90D	USB	USB_EXT_A_MUXED_P	
		USB_90D	USB	USB_EXT_A_MUXED_N	
	USB_MINI	USB_90D	USB	USB_MINI_P	9 20
		USB_90D	USB	USB_MINI_N	9 20
	USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
		USB_90D	USB	USB_EXTD_N	9 20
	USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 31
		USB_90D	USB	USB_CAMERA_N	20 31
	USB_BT	USB_90D	USB	USB_BT_P	20 31
		USB_90D	USB	USB_BT_N	20 31
	USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
		USB_90D	USB	USB_TPAD_N	20 50
	USB_IR	USB_90D	USB	USB_IR_P	20 41
		USB_90D	USB	USB_IR_N	20 41
	USB_EXTB	USB_90D	USB	USB_EXTB_P	20 40
		USB_90D	USB	USB_EXTB_N	20 40
	USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 32
		USB_90D	USB	USB_EXCARD_N	20 32
	USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
		USB_90D	USB	USB_EXTC_N	9 20
	MCP_USB_RBIA5	MCP_USB_RBIA5		MCP_USB_RBIA5_GND	20
	SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21
	SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 45
	SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 45
	SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 45
	HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
		HDA_55S	HDA	HDA_BIT_CLK_R	21
	HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 54
		HDA_55S	HDA	HDA_SYNC_R	
	HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
		HDA_55S	HDA	HDA_RST_L	21 54
	HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 54
		HDA_55S	HDA	HDA_SDIN_CODEC	
	HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 54
		HDA_55S	HDA	HDA_SDOUT_R	21
	MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
	MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
		CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
	SPT_CLK	SPT_55S	SPT	SPI_CLK_R	21 44
		SPT_55S	SPT	SPI_CLK	44 53
	SPT_MOSI	SPT_55S	SPT	SPI_MOSI_R	21 44
		SPT_55S	SPT	SPI_MOSI	44 53
	SPT_MISO	SPT_55S	SPT	SPI_MISO	21 44
		SPT_55S	SPT	SPI_MISO_R	53
	SPT_CS0	SPT_55S	SPT	SPI_CS0_R_L	21 44
		SPT_55S	SPT	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=MUXGFX	SYNC_DATE=02/18/2008
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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

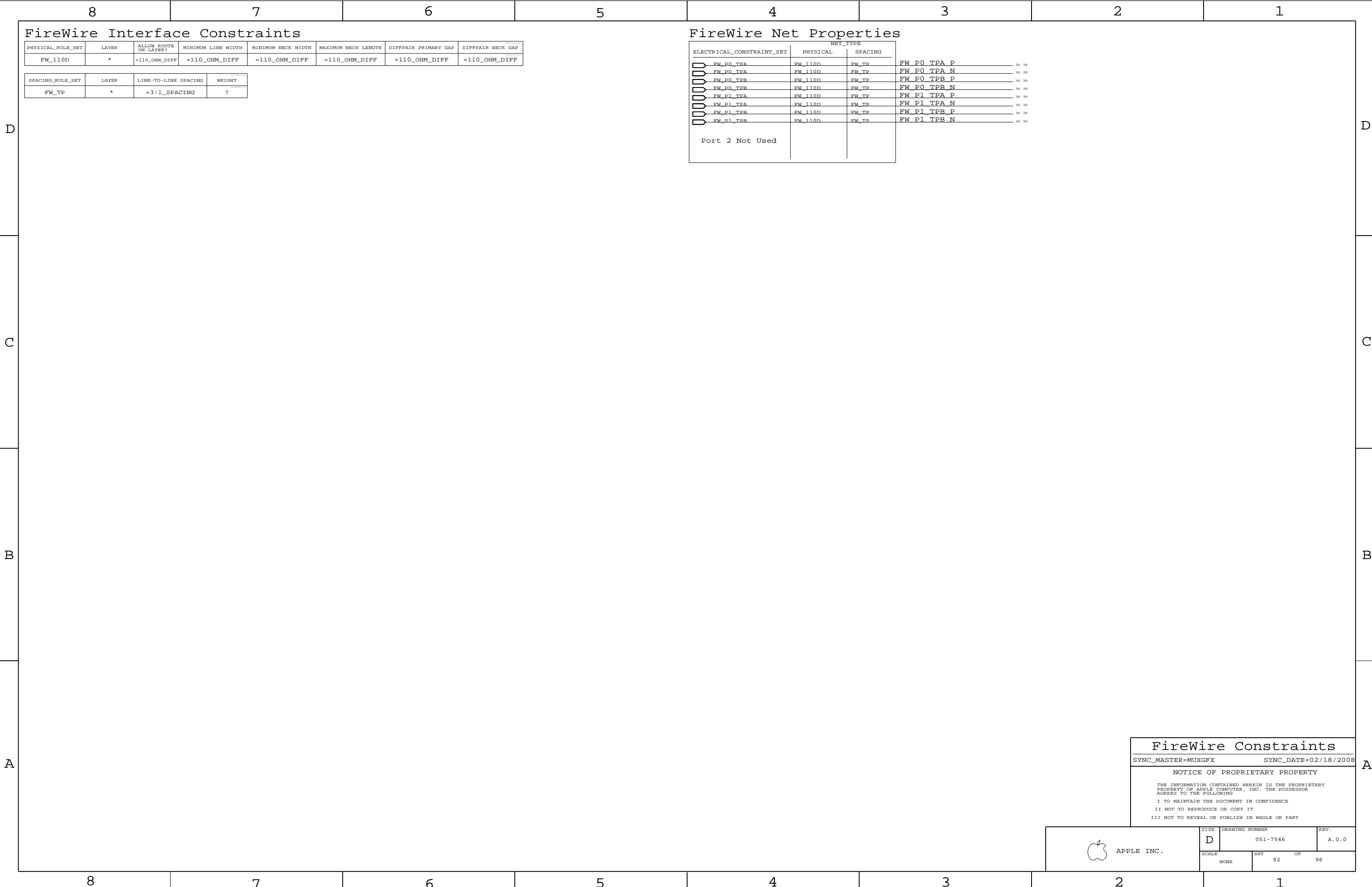
88E1116R (Ethernet PHY) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
<input type="checkbox"/>	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD	10
<input type="checkbox"/>	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND	10
<input type="checkbox"/>	MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R	10 34
<input type="checkbox"/>		ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1	33 34
<input type="checkbox"/>	ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET INTR L	
<input type="checkbox"/>	ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO	10 33
<input type="checkbox"/>	ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC	10 33
<input type="checkbox"/>	ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET PWRDWN L	
<input type="checkbox"/>		ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R	10 33
<input type="checkbox"/>	ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK	33
<input type="checkbox"/>		ENET_MII_55S	ENET_MII	ENET RXD R<3..0>	33
<input type="checkbox"/>	ENET_RXD	ENET_MII_55S	ENET_MII	ENET RXD<0>	33
<input type="checkbox"/>	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<3..1>	10 33
<input type="checkbox"/>	ENET_RXD	ENET_MII_55S	ENET_MII	ENET RX CTRL	10 33
<input type="checkbox"/>	ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK	10 33
<input type="checkbox"/>	ENET_TXD0	ENET_MII_55S	ENET_MII	ENET TXD<0>	10 33
<input type="checkbox"/>	ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<3..1>	10 33
<input type="checkbox"/>	ENET_TXD	ENET_MII_55S	ENET_MII	ENET TX CTRL	10 33
<input type="checkbox"/>		ENET_MII_55S	ENET_MII	ENET RESET L	10 33
<input type="checkbox"/>	ENET_MDI	ENET_MDI_100M	ENET_MDI	ENET MDI P<3..0>	33 35
<input type="checkbox"/>		ENET_MDI_100M	ENET_MDI	ENET MDI N<3..0>	33 35



D

C

B

A

D

C

B

A

8		7			6		
GDDR3 Frame Buffer Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.















MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	PHYSICAL	SPACING			
FE00	LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	80 83
FE00	LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	80 83
FE00	LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA P<2..0>	80 83
FE00	LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA N<2..0>	80 83
FE00	LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	80 83
FE00	LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	80 83
FE00	LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA P<2..0>	80 83
FE00	LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA N<2..0>	80 83
FE00		LVDS_100D	LVDS	LVDS_CONN A CLK F P	7 79
FE00		LVDS_100D	LVDS	LVDS_CONN A CLK F N	7 79
FE00		LVDS_100D	LVDS	LVDS_CONN B CLK F P	7 79
FE00		LVDS_100D	LVDS	LVDS_CONN B CLK F N	7 79
FE00		LVDS_100D	LVDS	LVDS_CONN A CLK P	79 80
FE00		LVDS_100D	LVDS	LVDS_CONN A CLK N	79 80
FE00		LVDS_100D	LVDS	LVDS_CONN A DATA P<2..0>	7 79 80
FE00		LVDS_100D	LVDS	LVDS_CONN A DATA N<2..0>	7 79 80
FE00		LVDS_100D	LVDS	LVDS_CONN B CLK P	79 80
FE00		LVDS_100D	LVDS	LVDS_CONN B CLK N	79 80
FE00		LVDS_100D	LVDS	LVDS_CONN B DATA P<2..0>	7 79 80
FE00		LVDS_100D	LVDS	LVDS_CONN B DATA N<2..0>	7 79 80
FE00	DP_ML	DP_100D	DISPLAYPORT	DP_ML C P<3..0>	81
FE00		DP_100D	DISPLAYPORT	DP_ML C N<3..0>	81
FE00	DP_ML	DP_100D	DISPLAYPORT	DP_ML P<3..0>	80 81
FE00		DP_100D	DISPLAYPORT	DP_ML N<3..0>	80 81
FE00	DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN P<3..0>	81
FE00		DP_100D	DISPLAYPORT	DP_ML_CONN N<3..0>	81
FE00	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH C P	80 81
FE00	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH C N	80 81

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_A_CLK_P	cmpr3_80n	cmpr3_clk	FB A CLK P<0>	72 73
FB_B_CLK_P	cmpr3_80n	cmpr3_clk	FB A CLK N<0>	72 73
FB_B_CLK_P	cmpr3_80n	cmpr3_clk	FB A CLK P<1>	72 73
FB_B_CLK_P	cmpr3_80n	cmpr3_clk	FB A CLK N<1>	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A MA<1..0>	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A MA<12..6>	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A BA<2..0>	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A RAS L	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A CAS L	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A WE L	72 73
FB_AB_CMD_RDN	cmpr3_40b555r	cmpr3_cmd	FB A CE	72 73
FB_AB_CMD	cmpr3_40b555r	cmpr3_cmd	FB A CS0 L	72 73
FB_AB_CMD_RDN	cmpr3_40b555r	cmpr3_cmd	FB A DRAM RST	72 73
FB_A_CMD	cmpr3_40sr	cmpr3_cmd	FB A LMA<5..2>	72 73
FB_B_CMD	cmpr3_40sr	cmpr3_cmd	FB A UMA<5..2>	72 73
FB_A_WDQS0	cmpr3_40sr	cmpr3_pqs	FB A WDQS<0>	72 73
FB_A_WDQS1	cmpr3_40sr	cmpr3_pqs	FB A WDQS<1>	72 73
FB_A_WDQS2	cmpr3_40sr	cmpr3_pqs	FB A WDQS<2>	72 73
FB_A_WDQS3	cmpr3_40sr	cmpr3_pqs	FB A WDQS<3>	72 73
FB_A_RDQS0	cmpr3_40sr	cmpr3_pqs	FB A RDQS<0>	72 73
FB_A_RDQS1	cmpr3_40sr	cmpr3_pqs	FB A RDQS<1>	72 73
FB_A_RDQS2	cmpr3_40sr	cmpr3_pqs	FB A RDQS<2>	72 73
FB_A_RDQS3	cmpr3_40sr	cmpr3_pqs	FB A RDQS<3>	72 73
FB_A_DQ_BYTE0	cmpr3_40sr	cmpr3_data	FB A DQ<7..0>	72 73
FB_A_DQ_BYTE1	cmpr3_40sr	cmpr3_data	FB A DQ<15..8>	72 73
FB_A_DQ_BYTE2	cmpr3_40sr	cmpr3_data	FB A DQ<23..16>	72 73
FB_A_DQ_BYTE3	cmpr3_40sr	cmpr3_data	FB A DQ<31..24>	72 73
FB_A_DQM0	cmpr3_40sr	cmpr3_data	FB A DQM L<0>	72 73
FB_A_DQM1	cmpr3_40sr	cmpr3_data	FB A DQM L<1>	72 73
FB_A_DQM2	cmpr3_40sr	cmpr3_data	FB A DQM L<2>	72 73
FB_A_DQM3	cmpr3_40sr	cmpr3_data	FB A DQM L<3>	72 73
FB_B_WDQS0	cmpr3_40sr	cmpr3_pqs	FB B WDQS<4>	72 73
FB_B_WDQS1	cmpr3_40sr	cmpr3_pqs	FB B WDQS<5>	72 73
FB_B_WDQS2	cmpr3_40sr	cmpr3_pqs	FB B WDQS<6>	72 73
FB_B_WDQS3	cmpr3_40sr	cmpr3_pqs	FB B WDQS<7>	72 73
FB_B_RDQS0	cmpr3_40sr	cmpr3_pqs	FB B RDQS<4>	72 73
FB_B_RDQS1	cmpr3_40sr	cmpr3_pqs	FB B RDQS<5>	72 73
FB_B_RDQS2	cmpr3_40sr	cmpr3_pqs	FB B RDQS<6>	72 73
FB_B_RDQS3	cmpr3_40sr	cmpr3_pqs	FB B RDQS<7>	72 73
FB_B_DQ_BYTE0	cmpr3_40sr	cmpr3_data	FB B DQ<39..32>	72 73
FB_B_DQ_BYTE1	cmpr3_40sr	cmpr3_data	FB B DQ<47..40>	72 73
FB_B_DQ_BYTE2	cmpr3_40sr	cmpr3_data	FB B DQ<55..48>	72 73
FB_B_DQ_BYTE3	cmpr3_40sr	cmpr3_data	FB B DQ<63..56>	72 73
FB_B_DQM0	cmpr3_40sr	cmpr3_data	FB B DQM L<4>	72 73
FB_B_DQM1	cmpr3_40sr	cmpr3_data	FB B DQM L<5>	72 73
FB_B_DQM2	cmpr3_40sr	cmpr3_data	FB B DQM L<6>	72 73
FB_B_DQM3	cmpr3_40sr	cmpr3_data	FB B DQM L<7>	72 73

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	CKE655_D0736E	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 76
	CK55S_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS 76
	LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P 77
	LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N 77
	LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0> 77
	LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0> 77
	LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0> 77
	LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0> 77
	DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0> 77
	DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0> 77
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P 77
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N 77
		DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P 80
		DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N 80

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
FB_C_CLK_0	nmn03_50N	nmn03_CTK	FB_B_CLK_P<0>
FB_C_CLK_0	nmn03_50N	nmn03_CTK	FB_B_CLK_N<0>
FB_C_CLK_0	nmn03_50N	nmn03_CTK	FB_B_CLK_P<1>
FB_C_CLK_0	nmn03_50N	nmn03_CTK	FB_B_CLK_N<1>
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_MA<1..0>
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_MA<12..6>
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_RA<2..0>
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_RAS_L
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_CAS_L
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_WE_L
FB_CD_CMD_RD	nmn03_40R55SE	nmn03_CMD	FB_B_CKE
FB_CD_CMD	nmn03_40R55SE	nmn03_CMD	FB_B_CS0_L
FB_CD_CMD_RD	nmn03_40R55SE	nmn03_CMD	FB_B_DRAM_RST
FB_C_CMD	nmn03_40SE	nmn03_CMD	FB_B_IMA<5..2>
FB_C_CMD	nmn03_40SE	nmn03_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	nmn03_40SE	nmn03_PQS	FB_B_WDQS<0>
FB_C_WDQS1	nmn03_40SE	nmn03_PQS	FB_B_WDQS<1>
FB_C_WDQS2	nmn03_40SE	nmn03_PQS	FB_B_WDQS<2>
FB_C_WDQS3	nmn03_40SE	nmn03_PQS	FB_B_WDQS<3>
FB_C_RDQS0	nmn03_40SE	nmn03_PQS	FB_B_RDQS<0>
FB_C_RDQS1	nmn03_40SE	nmn03_PQS	FB_B_RDQS<1>
FB_C_RDQS2	nmn03_40SE	nmn03_PQS	FB_B_RDQS<2>
FB_C_RDQS3	nmn03_40SE	nmn03_PQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	nmn03_40SE	nmn03_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	nmn03_40SE	nmn03_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	nmn03_40SE	nmn03_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	nmn03_40SE	nmn03_DATA	FB_B_DQ<31..24>
FB_C_DQM0	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<0>
FB_C_DQM1	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<1>
FB_C_DQM2	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<2>
FB_C_DQM3	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	nmn03_40SE	nmn03_PQS	FB_B_WDQS<4>
FB_D_WDQS1	nmn03_40SE	nmn03_PQS	FB_B_WDQS<5>
FB_D_WDQS2	nmn03_40SE	nmn03_PQS	FB_B_WDQS<6>
FB_D_WDQS3	nmn03_40SE	nmn03_PQS	FB_B_WDQS<7>
FB_D_RDQS0	nmn03_40SE	nmn03_PQS	FB_B_RDQS<4>
FB_D_RDQS1	nmn03_40SE	nmn03_PQS	FB_B_RDQS<5>
FB_D_RDQS2	nmn03_40SE	nmn03_PQS	FB_B_RDQS<6>
FB_D_RDQS3	nmn03_40SE	nmn03_PQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	nmn03_40SE	nmn03_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	nmn03_40SE	nmn03_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	nmn03_40SE	nmn03_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	nmn03_40SE	nmn03_DATA	FB_B_DQ<63..56>
FB_D_DQM0	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<4>
FB_D_DQM1	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<5>
FB_D_DQM2	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<6>
FB_D_DQM3	nmn03_40SE	nmn03_DATA	FB_B_DQM_L<7>

GPU (G96) Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	14 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE: From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PCB Rule Definitions	
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